Final Assessment of Demonstrator Concept and Implementation

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Abstract:
"This deliverable provides a comparison of SoTA OFDM and the proposed non-orthogonal PHY design with respect to the KPIs. An outcome will be the evaluation and quantification, to which extent the expected advantages of non-orthogonal modulation (e.g. robustness) could be shown under realistic side conditions. The deliverable will conclude on critical implementation components for asynchronous 5G systems, which might become a showstopper for practical application."

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Executive Summary

This deliverable presents the final set of transceiver algorithm implementations developed according to WP2-WP4 results. Particular focus is put on the description of the hardware and software platforms and analysis of algorithms from an implementation perspective. The outcome of this document is the evaluation and quantification, to which extent the expected advantages of non-orthogonal modulation could be shown under realistic side conditions.

1 Introduction

5th generation (5G) mobile networks are expected to be denser and increasingly heterogeneous with respect to traffic types – machine type communication (MTC) generating a few bytes/s vs. HD video demanding several hundred Mbytes/s, network architecture – supporting femto-, pico-, micro- and macro-cells, and in terms of spectrum usage (aggregation of fragmented spectrum). Ensuring completely orthogonal wireless access becomes costly or even impossible, hence robust modulation schemes with a confined spectral response beyond OFDM may be a solution.

5GNOW proof-of-concept work package (WP5) concentrate efforts in developing demonstrations to highlight specific aspects of new PHY proposals. In this deliverable FBMC and GFDM prototypes developed by CEA and TUD are presented in details, their demonstrators exhibited at VTC Spring 2013, FUNEMS 2013 and EuCNC'14 (Figure 1-1) have shown that more localized spectrum can be flexibly obtained through the use of filtered multicarrier approach at an affordable hardware complexity. The idea is to explore the new PHY properties together with more flexible MAC layer concepts, addressing distinct types of traffic, from high data rate bit pipe to sporadic and asynchronous low rate access.

The document presents scenarios and the demonstrated use cases as well its related PHY parameters. It starts with an overall description of the used hardware setup as well as the final set of transceiver algorithms and control functionality for single- and multi-user transmission according to the WP2-4 input. The deliverable then describes the evaluation of the HW demonstrator concept and eventually concludes on the critical implementation components for asynchronous 5G systems.

Figure 1-1: VTC Spring 2013 and FUNEMS 2013 5GNOW booths (top); EuCNC'14 5GNOW booth (bottom)

2 Scenarios, PHY parameters and KPIs

Synchronizing cooperative networks is expensive or even impossible. The problem will become tremendously more challenging when considering low-cost micro and femto base station deployments or even lower-cost sensor devices, which may transmit without synchronizing to the network's clock. However, the current LTE modulation technique "OFDMA" can only operate if strict time and frequency synchronization between users and a base station is achieved. Distributed transmission techniques, such as CoMP, impose the even more stringent requirement of synchronous base stations on top.

In addition, future 5G networks will have to ensure efficient and therefore flexible use of scarce and fragmented spectral resources. Carrier aggregation, inter-band as well as intra-band, call for new transceiver architectures are to be realized. In addition, non-contiguous spectrum aggregation poses extreme challenges on achieving blocking requirements and on satisfying regulatory out-of-band spectrum constraints. This cannot be achieved by the spectrum shape of OFDM, but requires a new modulation concept along with new hardware (e.g., wide-band A/D conversion) and signal processing approaches.

Understanding the limits of state-of-the-art OFDM and exploring / comparing the benefits of GFDM and FBMC in that regard, is part of the work package demonstrator in 5GNOW project.

2.1 Reference scenarios

The research of new PHY's in 5GNOW aims to offer scalable and spectrally malleable modulations that are attractive for 5G requirements, especially addressing non-orthogonal and asynchronous principles within the trinity of the corner scenarios MTC (machine-type communication), CoMP/HetNet, carrier aggregation, and Tactile Internet (extreme low latency requirements, roundtrip in the order of 1ms). The research proposal will make use of the natural emerging technological possibilities suitable for 5G communication and to better disseminate the ideas, proof of concepts by prototyping are of great interest, especially to show that the issue of complexity can be contoured in software defined radio platforms.

From the mentioned scenarios in D2.1 and D3.1 the fragmented spectrum will be especially explored in this report. The provision of carrier aggregation/fragmented spectrum transmission techniques using non-orthogonal waveforms with relaxed synchronization requirements will be demonstrated in terms of increased bandwidth efficiency in white spaces.

As a GFDM setup from TUD side the demonstrator will use the National Instruments HW platform NI-PXI-7965 to approach the implementation challenge in steps. The main goal is to close the gap between research and implementation based on built-drivers and available examples from the platform. As a schematic example the GFDM single-link prototype has followed 3 steps:

Step 1: Matrix model off-line simulator
Step 2: Real-time based application
Step 3: Increased throughput implementation using FPGA

From CEA LETI side the demonstration is based on a custom evaluation board to address the implementation of FBMC in a range of frequencies below 1GHz. Other ranges of frequencies are explored using NI HW as up/down converter.

Figure 2-1 and Figure 2-2 detail a bit the step approach in terms of single link and multi-user/parallel links desired in the end of the project.

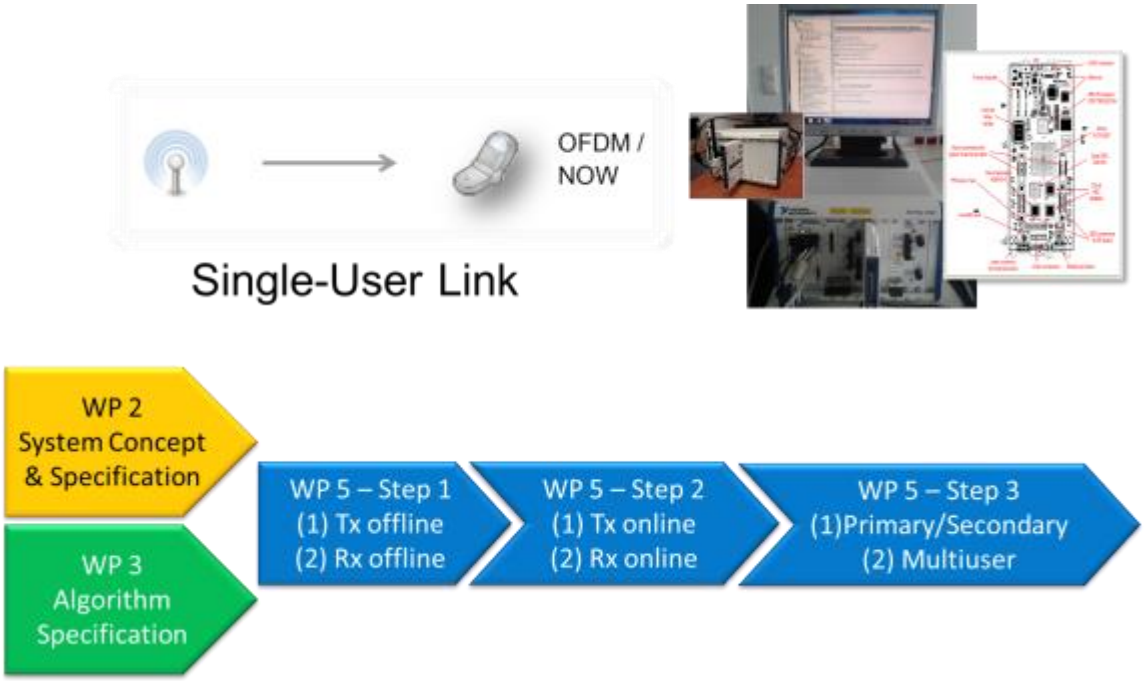


Figure 2-1: Single-link PHY prototyping approach

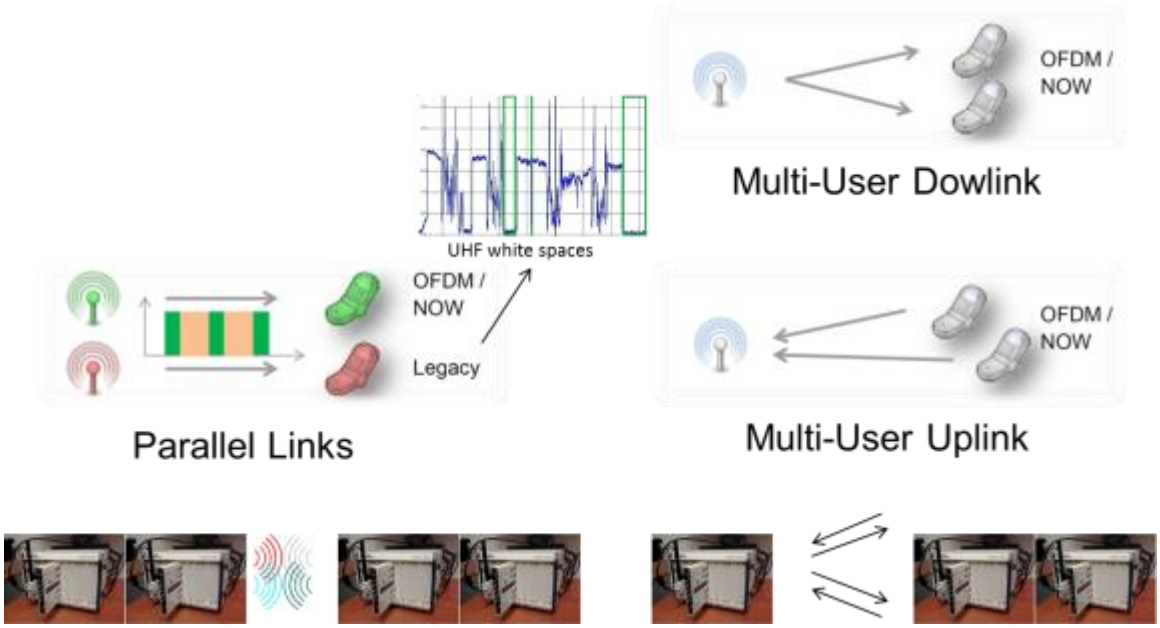


Figure 2-2. Multi-user/parallel-link PHY prototyping approach

2.2 Low latency

A major ingredient for designing new 5G killer applications is to be able to achieve a round-trip latency of the order of 1 ms, from sensors through the 5G air interface to the control server, and back to a wirelessly connected actor. This results in a latency budget for the air interface on the order of 0.1 ms, which is in the same ball park as the duration of one single OFDM symbol of LTE. Considering framing, and deframing as well as FEC (forward error correction), it becomes clear that LTE's current OFDMA specification cannot be used to address real time interaction systems on top of current applications in a 5G PHY. Thus, a new channel access scheme will be required to implement low latency data connections.

The requirements of low latency motivated and summarized in [Fet12], call for a new air interface beyond OFDM. The development of flexible, robust waveforms and their extension towards multi-antenna techniques will be one of the key research areas during the next years. Among others, GFDM is a non-orthogonal modulation technique that has been researched to address multiple of the above-mentioned issues of OFDM.

Similar to OFDM, GFDM is a multicarrier transmission technique that can make use of non-orthogonal subcarriers. Low out-of-band radiation is achieved by filtering multiple consecutive symbols on each subcarrier, with use of non-continuous bandwidth by just enabling or not a set of subcarriers. GFDM differs from FBMC due its block based data implementation, shortening the transmission length using tail biting filtering of each subcarrier and allowing the efficient use of cyclic prefix (CP) and suffix (CS). With flexible time and frequency slots the GFDM transceiver will be designed having the challenges in mind of the low latency in the Tactile Internet scenario. More details about it can be found in the 5GNOW deliverables D2.1 and D3.1. One possible GFDM reference scenario specification is reproduced below.

Simulation Parameter	Value
Subcarrier spacing Δf	240kHz (with 16 symbols per sub-carrier*)
Subcarriers per "PRB"	1
FFT size	256
No. of used "PRBs"	10*
Block (=subframe) duration	1/240k * 16 = 67us
Modulation	64QAM
GFDM CP-length	1 symbol of the subcarrier, 1/240k=~4us
Receiver	MF, ZF or MMSE
Channel	AWGN / Veh A block fading
Freq. offset (*)	[0 … 0.1Δf]
Timing offset	[0 … 0.1Ts]

"LTE- like" format for 2.5MHz bandwidth 256 points IFFT with sample rate 3.84 Msamples/s)

*Approximately 16 slots * 6bits each*10 subcarriers allocation = 960 bits (<100µs burst)

Figure 2-3: GFDM Reference Scenario Specification

The focus of the GFDM reference scenario refers to uplink MTC communication. The cell size considered in the scenario is around 1km in ratio, so multipath in the order of less than 4µs duration is expected (1µs delay corresponds to 300 meters deviation). The scenario includes low effort in synchronism and the transmission of data in bursts of 1kbit in at most 100 µs (thus at a rate of 10 Mbit/s). Due to the "low effort" in synchronism (10 ppm) at the receiver "poor" synchronicity in frequency together with the effect of propagation delay and delay spread occurs (few µs, up to guard interval). The 10 ppm corresponds to a frequency offset of 0.1 Δf.

The motivation for the reference scenario is to investigate how well "asynchronicity" can be supported in a MTC setting with the GFDM approach. Timing and frequency offsets are also treated in the scenario. The total frequency offsets are caused by the M2M transmitters, while the BTS are synchronised. Further, for MTC the relaxed oscillator requirements are expected to be beneficial in terms of not only price, but also in terms of the settling time required for awakening of a device in sleep mode.

Another important aspect to consider is if this new waveform can be compatible with the previous generation master clock rate. In the LTE case the corresponding clock relation to WCDMA is 3.84 MHz x 8 = 30.72 MHz. So a LTE-compatible 5G PHY based on GFDM would be also of interest. In the next tables two set of possible arrangements are presented considering a LTE grid in the frequency division duplexing (FDD) mode.

Parameter	Normal mode	Extended mode
Frame duration	10 ms or 307.200 samples	
Subframe duration	1 ms or 30.720 samples	
Slot duration	0.5 ms or 15.360 samples	
Subcarrier spacing	15 kHz	
Subcarrier bandwidth	15 kHz	
Sampling freq. (clock)	30.72 MHz	
# of subcarriers	2048	
# of active subcarriers	1200	
Resource block	12 subcarriers of one slot	
Number of OFDM per slot	7	6
CP length (samples)	First symbol: 160 Other symbols: 144	512

(a)

Parameter	Normal mode
Subframe duration	1 ms or 30.720 samples
GFDM symbol duration	66.67μs or 2048 samples
Subsymbol duration	4.17μs or 128 samples
Subcarrier spacing	240 kHz
Subcarrier bandwidth	240 kHz
Sampling freq. (clock)	30.72 MHz
Subcarrier spacing factor N	128
subsymbol spacing K	128
# active subcarriers N_{on}	75
# subsymbols per GFDM symbol M	15
# GFDM symbols per subframe	15
CP length	4.17μs or 128 samples
Prototype filter	Dirichlet

(b)

Parameter	Normal mode
Subframe duration	1 ms or 30.720 samples
GFDM symbol duration	50 μs or 1536 samples
Subsymbol duration	3.125 μs or 96 samples
Subcarrier spacing	360 kHz
Subcarrier bandwidth	320 kHz
Sampling freq. (clock)	30.72 MHz
Subcarrier spacing factor N	256/3
Subsymbol spacing K	96
# active subcarriers N_{on}	half of available RBs
# subsymbols per GFDM symbol M	15
# GFDM symbols per subframe	20
CP length	3.125μs or 96 samples
Prototype filter	Dirichlet

(c)

Figure 2-4: (a) LTE parameter for the FDD mode, (b) GFDM configuration aligned with the LTE grid, (c) GFDM parameters for asynchronous signalling

Algorithm processing complexity issues will be presented in further sections about the GFDM demonstrator.

2.3 Multi-user fragmented spectrum access

The advent of the Digital Agenda and the introduction of carrier aggregation are forcing the transmission systems to deal with fragmented spectrum. 3GPP/LTE-A is already dealing with some spectrum agility as a requisite to allow worldwide interoperability of devices in a fragmented spectrum. In this context, the scenario under consideration is UL asynchronous multi-user access on fragmented spectrum for 5G with non-orthogonal waveform. The objective is to allow relaxing both time/frequency synchronization constraints while enabling flexible fine-grained sharing of fragmented spectrum. If the spectral needs are not met in a contiguous space of spectrum, then some form of aggregation should be realized. The specific nature of the fragmented spectrum and the stringent requirements on adjacent band leakage are suggesting a new approach for the PHY using filter bank modulation (FBMC) and spectrum pooling techniques.

Both OFDM and FBMC may theoretically be suited to multicarrier-based spectrum pooling. However, high adjacent channels' rejection cannot be met without a very complex and programmable band-pass transmit filter in the CP-OFDM case, whereas FBMC would simply requires "switching on and off" the appropriate carriers at the transmitter. The main shortcoming of the OFDM waveform identified here originates from the large side-lobes because of the rectangular shaping of the temporal signal whereas the FBMC built-in filtering feature adapts to spectrum availability even in the fragmented case.

Despite its prominence in modern broadband radios, CP-OFDM has some drawbacks for the intended scenario operation. Indeed, CP-OFDM side lobes make it inappropriate in adjacent channels, unless expensive rejection filters are used. Spectrum pooling is an appealing approach to virtually elaborate wider channels, but again CP-OFDM is not applicable because of unaffordable out-of-band leakage. FBMC is as a valid alternative to CP-OFDM, as it achieves both adjacent coexistence and spectrum pooling. Figure 2-5 illustrates the scenario which comprises one base station and 2 users while Figure 2-6 summarizes the most important parameters.

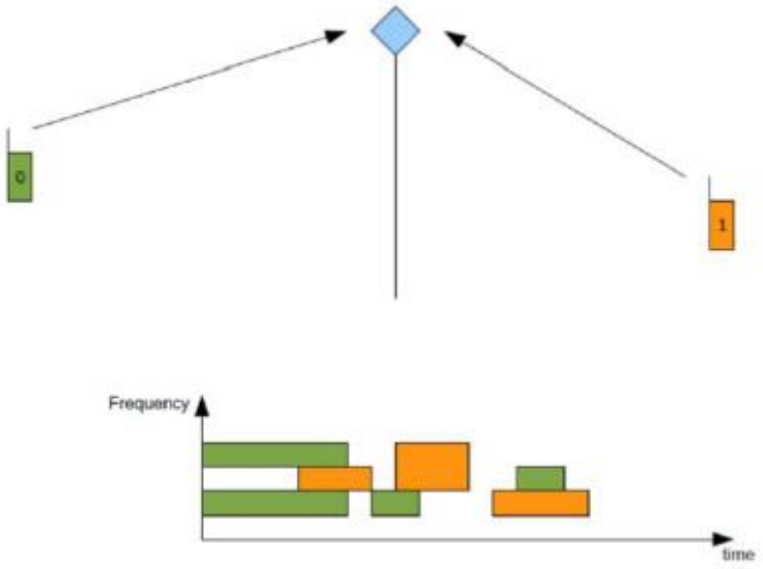


Figure 2-5: Multi User UL Reference Scenario for Fragmented Spectrum with FBMC

The FBMC TRX demonstrator PHY parameters are derived from the LTE format for 10MHz bandwidth with sampling rate 15.36MHz. The following section describes the considered parameters.

Simulation Parameter	Value	
Subcarrier spacing Δf	15 kHz	LTE format for 10 MHz bandwidth with sampling rate 15.36 MHz
Subcarriers per PRB	12 p	
FFT size	1024	
No. of used carriers	12 to 501 (depending on p)	
No. of used PRBs	configurable	
Block (subframe) duration	1.6 ms	
FBMC Filter	K=4 (optimized for ACLR)	
Modulation	QPSK to 64-QAM	Adaptative data rate
Coding rate	1/2, 2/3, 3/4 (CC K=7)	
OFDM CP-length	N/A	
Performance metric	(BER,PER) vs SNR (/Freq offset & Timing Offset)	

Figure 2-6: UL MU Fragmented Spectrum Reference Scenario Specification

2.4 KPIs

The KPI's under consideration for the scenarios are the out of band radiation, known as Adjacent Channel Leakage Ratio (ACLR), and the required level of synchronization, in terms of parts per million (ppm) precision of the oscillators.

Other aspects as Modulation Error Ratio (MER) and peak to average power ratio (PAPR) will be used to construct metrics to evaluate the performance of the waveforms. Also the flexibility of the resource grid and efficient use of time and frequency in packets as short as possible are of interest. These characteristics will be tuned to adapt the transmission to diverse conditions and applications. The adjustable spectral properties will be defined with the variation of the shape of subcarrier filter and additional time windowing function. The use of less subcarriers with larger bandwidth and the shape of subcarrier filter will be checked to try to improve PAPR, avoiding spikes in signal amplitude.

The following picture captures some of the mentioned features for GFDM.

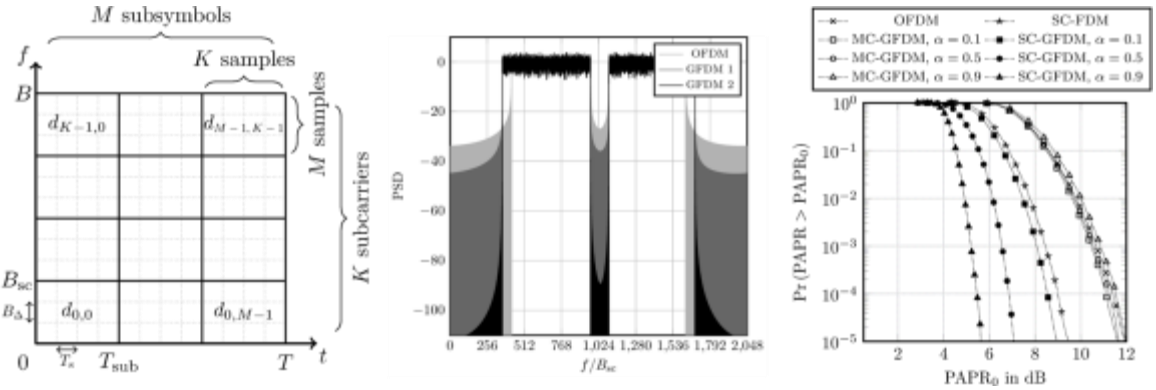


Figure 2-7: GFDM grid resources, out of band radiation and PAPR

3 Considered platforms

3.1 NI PXI Platform for prototyping RF technologies

3.1.1 Platform Overview

PXI (PXI/PXIe – PCI/PCIe eXtension for Instrumentation) is a rugged PC-based platform for measurement and automation systems. PXI combines PCI electrical-bus features with the modular, Eurocard packaging of CompactPCI and then adds specialized synchronization buses and key software features. PXI is both a high-performance and low-cost deployment platform for applications such as manufacturing test, military and aerospace, machine monitoring, automotive, and industrial test. Developed in 1997 and launched in 1998, PXI is open industry standard governed by the PXI Systems Alliance (PXISA), a group of more than 70 companies chartered to promote the PXI standard, ensure interoperability, and maintain the PXI specification.

As the backbone of the PXI system, the chassis provides the power, cooling, and communication buses of PCI and PCI Express for the controller and modules. PXI chassis are available in a variety of configurations such as low noise, high temperature, and low- to high-slot count. They also offer a range of I/O module slot types, integrated peripherals such as LCD displays and others.

Figure 3-1: PXI System

PCI Express provides a point-to-point bus topology, this gives each device its own direct access to the bus, and thus its own dedicated data pipelines called lanes. It is possible to group these lanes together to increase bandwidth to the slot to achieve up to 4 GB/s of throughput, or 8 GB/s with 2nd generation (Gen2) PCIe compatible devices.

PXI builds on its CompactPCI architecture base by adding integrated timing and synchronization that is used to route synchronization clocks and triggers internally. PXI chassis incorporates a dedicated 10 MHz system reference clock, PXI trigger bus, star trigger bus, and slot-to-slot local bus, while a PXI Express chassis adds a 100 MHz differential system clock, differential signalling, and differential star triggers to address the need for advanced timing and synchronization.

The PXI specification requires a minimum of 25 W of power be available to each peripheral slot, while the PXI Express specification requires a minimum of 30 W, with each slot being able to dissipate the same amount of heat.

3.1.2 5GNOW hardware set

Based on the project requirements and initial experiments in the early stages of the project the system in Figure 3-2 was proposed for 5GNOW research demonstrations.

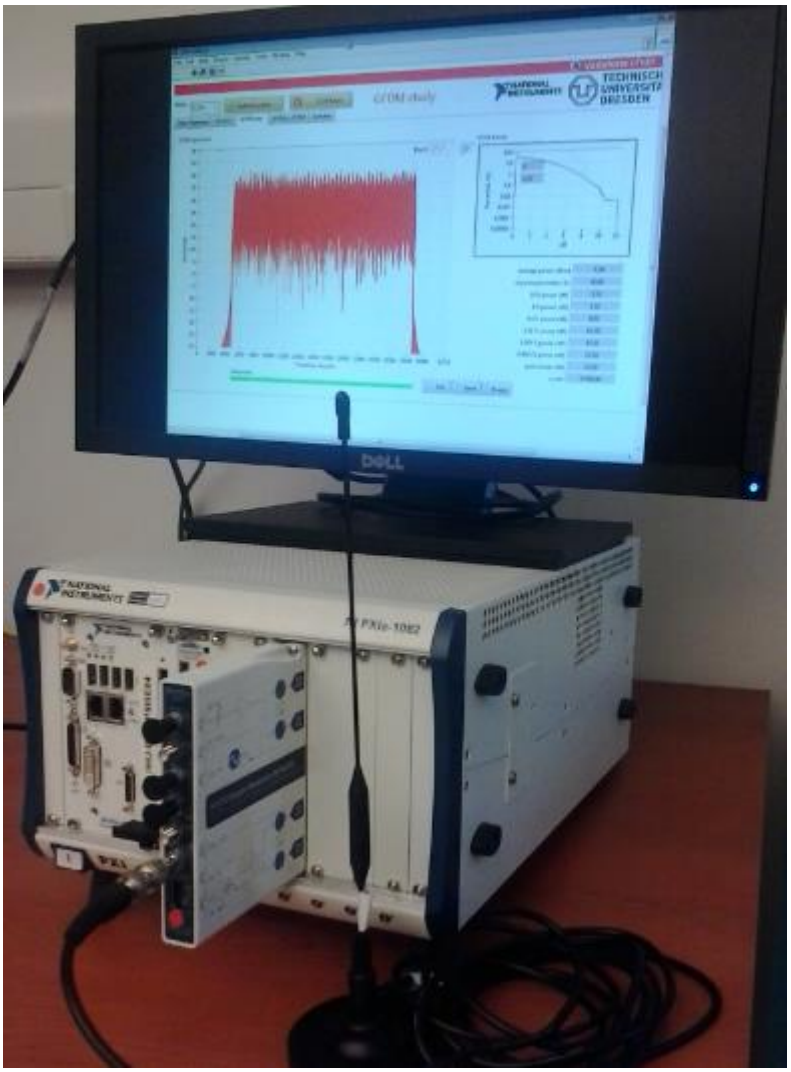


Figure 3-2. Hardware set at TUD, GFDM demo set

The hardware set consist four single PXI Express subsystems (Figure 3-3) which enables the demonstration of multi-user link capabilities with different quality of synchronization between subsystems. Each subsystem consists an 8-slot PXI Express high-performance chassis, an Intel i7 based high-performance controller for controlling the application and performing baseband processing on CPU, two FPGA (NI FlexRIO) modules for high-throughput baseband processing, one transceiver adapter module for signal up-conversion and down-conversion to and from radio frequencies.

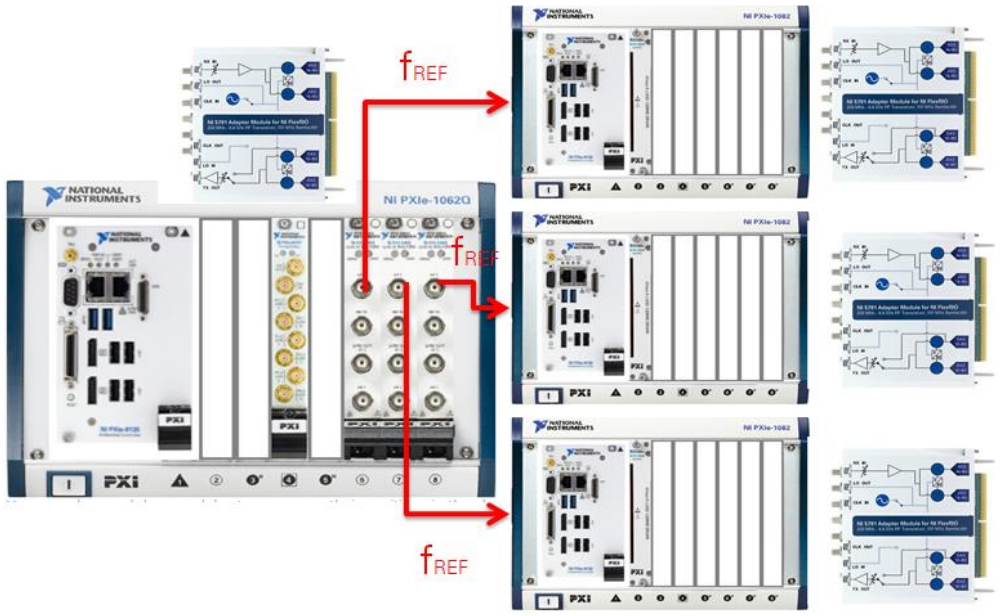


Figure 3-3: NI PXI Platfrom for 5GNOW

The RF Transceiver adapter module is attached to either FlexRIO, these units build up the RF Transceiver. The second FlexRIO acts as co-processor for the RF Transceiver, because FlexRIO boards can pass data to each other on the PXIe backplane with low latency (<10ns) and high throughput (800MBps), therefore this makes the systems scalable.

NI PXI Platform is highly flexible and programmable; this is why it is proper for algorithm prototyping. The most common way of programming it is using National Instruments LabVIEW development environment which uses graphical systems design concept for all the components: CPU based applications and embedded FPGA design.

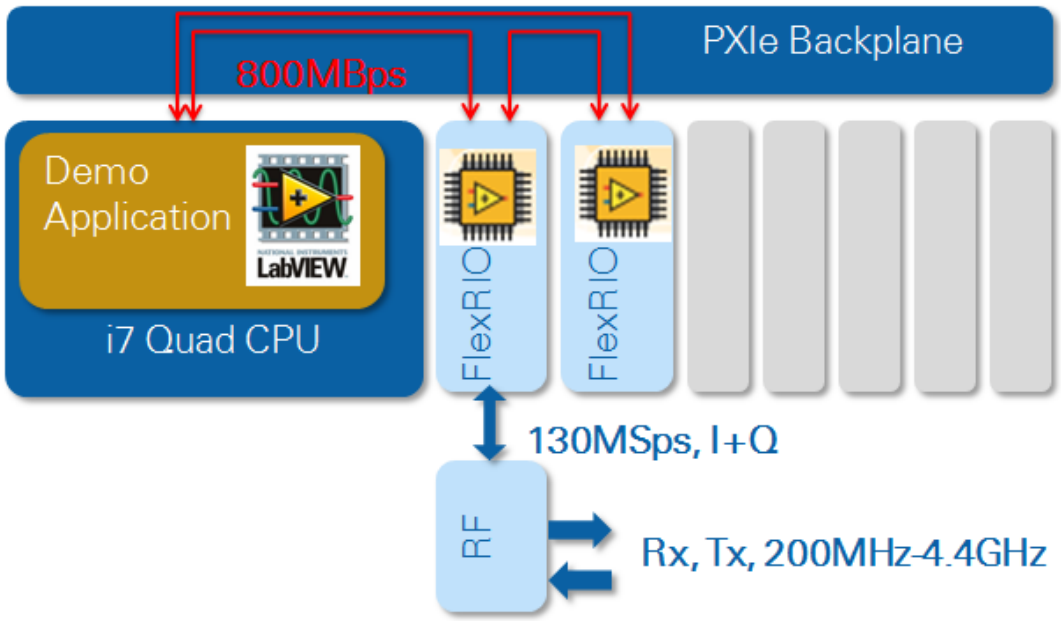


Figure 3-4: : Sub-module communication in a single chassis

3.1.2.1 NI PXIe-1082 chassis (3 of the 4 sub-systems; slave systems)

NI PXIe-1082 is an 8 slot chassis (1 for the controller and 7 for modules), all the slots have PXIe type, and some of them are PXI Hybrid compatible. Hybrid compatible slots can fit PCI cards and standard PXI cards which have hybrid compatible connector. Slot types are marked with glyphs on the front of the chassis with triangle, rectangle, circle respectively the controller, timing modules and any other modules.

Data throughput can be up to 3 GB/s to or from the controller. Peer-to-peer streaming between modules is up to 800MB/s unidirectional or ~760MB/s bidirectional.

3.1.2.2 NI PXIe-1062Q chassis (1 of the 4 sub-systems; master system)

NI PXIe-1062Q is also an 8 slot chassis, but not all the slots are PXIe. Slots 2-6-7-8 are normal PXI compatible. There are PXI modules in recent 5GNOW hardware set which are not PXIe Hybrid Compatible, therefore they can sit only in PXI slots. These cards are planned for timing and synchronization purposes. This is the reason why PXIe-1062Q was chosen for master chassis.

The colour of the slot glyphs shows the type of the slot: black is PXIe and white is PXI compatible.

Figure 3-5: NI PXIe-1062Q Chassis with 4 PXI slots and 3 PXIe(H) module slots

3.1.2.3 Intel-i7 Embedded Controller

PXI Chassis can be connected to remote computers as an extension of their PCI/PCIe buses and can be used with embedded controller (a rugged industrial computer with Intel based architecture).

Embedded controllers can run any kind of operating system which requires Intel architecture. Preinstalled controllers from NI usually run Windows (XP, XP FES, Win7 Pro) systems and/or NI Real-Time Operating System (NI RT). Due to the special BIOS settings on NI embedded controllers both of the OSes (Windows and RT) can be installed on the same hard disk (internal storage) and any of them can be chosen during the boot.

Due to present available and widely used virtualization technologies, both OSes can run in parallel by NI Hypervisor host virtualization system. NI Hypervisor is an option, not all the controllers have it installed.

In 5GNOW hardware set there are 4 PXIe-8133 controllers, 2 of them are delivered with Dual Boot option and the other 2 have NI Hypervisor installed.

Figure 3-6. PXIe-8133 Controller

NI PXIe-8133 with Dual Boot

NI PXIe-8133 is a Quad-Core Intel i7 based controller with up to 12 GB RAM and many interfaces, like USB 2.0, ExpressCard, GPIB, VGA/DVI-D, dual Gbit Ethernet, and with one 2.5" internal drive (HDD or SSD). In the current 5GNOW set controllers delivered with 4GB RAM and internal 250GB HDD. Dual boot controllers delivered with Windows 7 64 bit and NI RT operating system pre-installed. (Recovery partition is also part of the installation, therefore it is not recommended to re-partitioning the disk.)

NI PXIe-8133 with NI Hypervisor

NI Hypervisor enables the use of Windows and RT at the same time, sharing the hardware resources between those 2 systems. During the boot process it is possible to choose between booting up only Windows or Hypervisor (which starts Windows and RT as guest OSes).

This type of controllers Windows 7 32 bit is installed, because NI Hypervisor should be controlled administrated/configured by a Windows based client which can be installed only on 32 bit versions Windows.

There is a virtual network connection between the two guest operating systems. This allows handling the RT systems on the same way as from a remote Windows (developer) computer.

So the benefit of having this Hypervisor is to have the headless and real-time behavior on the embedded controller while accessing the development environment and host interface at the same time, without using external PC.

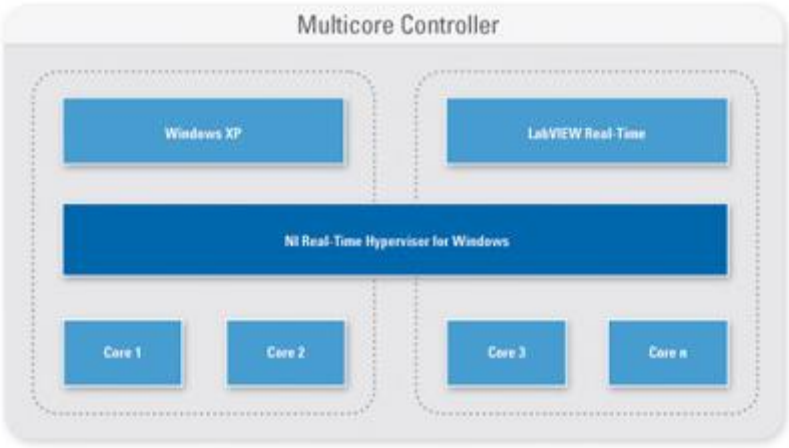


Figure 3-7. NI Hypervisor architecture

3.1.2.4 NI High-performance FPGA board: PXIe-7965R (FlexRIO)

The NI FlexRIO product family provides flexible, customizable I/O for NI LabVIEW FPGA. Solutions consist of NI FlexRIO FPGA Modules for PXI and PXI Express, and NI FlexRIO Adapter Modules, which add I/O to the FPGA. Together, they form a high-performance, reconfigurable instrument powered by LabVIEW FPGA. Adapter modules are available from NI and National Instruments Alliance, but 5GNOW partners can use the NI FlexRIO Module Development Kit (MDK) to build customized HW.

Figure 3-8. NI FlexRIO (PXIe-7965R)

3.1.2.5 RF Adapter Module: NI 5791 (FAM)

Interchangeable and customizable NI FlexRIO adapter modules define the physical inputs and outputs of an NI FlexRIO system.

The NI 5791 is an RF transceiver with continuous frequency coverage from 200 MHz to 4.4 GHz, with 100 MHz of instantaneous bandwidth on both TX and RX. It features a single-stage, direct conversion architecture, providing high bandwidth in the form factor of an NI FlexRIO adapter module. The

onboard synthesizer (local oscillator or LO) sets the center frequency for acquisition and generation, and can be exported to other modules for multiple-input, multiple-output (MIMO) synchronization. The LO can also be imported from an external connector, enabling synchronization of up to eight NI 5791 modules at up to 2.8 GHz without external amplification. For higher frequencies or a greater number of devices, an external LO distribution amplifier may be used.

The baseband analog-to-digital converters (ADCs) on the NI 5791 are 14-bit, clocked at 130 MS/s, to provide a sufficient excess rate for 100 MHz bandwidth after any digital signal processor (DSP) resampling and frequency shifts. Similarly, the digital-to-analog converter (DAC) has a 16-bit resolution and the data rate is 130 MS/s, which simplifies algorithm design. In a DSP on the DAC hardware, the data is subsequently interpolated four times to 520 MS/s before generation, which reduces out-of-band images. Direct access to raw ADC and DAC data on the NI FlexRIO FPGA module provides the ultimate flexibility in digital signal processing, data storage and streaming, and custom algorithm design for software defined radio (SDR), signal intelligence (SIGINT), streaming to and from disk, MIMO, beamforming, and other high-performance embedded RF applications. Additionally, the NI FlexRIO FPGA module and the PXI platform provide a means for ADC and DAC data synchronization, which is necessary for channel expansion. Twelve bidirectional digital I/O lines routed from the FPGA to a connector on the adapter module enable digital device under test (DUT) control and simple digital protocols. Examples for the NI 5791 are configured and compiled for only the NI PXIe-7966R and NI PXIe-7965R FPGA modules.

RF performance on the NI 5791 provides RX dynamic range greater than 105 dB, with a noise figure less than 8 dB at 2 GHz. The LO phase noise is better than 94 dBc/Hz at 2.4 GHz and a 10 kHz offset, and the loopback error vector magnitude (EVM) is less than 1.5 percent. All specifications are typical, and some require FPGA-based correction algorithms, which are provided in the form of example code.

Figure 3-9. NI 5791R

3.1.3 Synchronization possibilities for multi-user scenario

Since all the modules can be synchronized to PXI 10MHz reference clocks and multiple PXI chassis can be synchronized to each other with sharing references among them, therefore all the parties can be synchronized to all others (Figure 3-3).

Using signal generators (PXI-5406) in the master chassis it is possible to generate reference signals to the slaves in such a way that those can be tuned slightly different frequencies. With this implementation, artificial frequency error can be introduced to the system.

With control on the frequency errors it is possible to test and demonstrate the capabilities of the system in non-ideal, non-synchronized environment. Link robustness versus frequency error can be measured and compared between multiple transceiver/receiver algorithms.

PXI-5406 function generators provide 0.355Hz frequency resolution. PXIe-6674T Timing module is placed in the timing slot of the master chassis. This module is designed to discipline the reference clock in the master chassis to provide high stability clock (50 ppb) and enables the synchronization to external signal sources (GPS, IEEE 1588, or IRIG).

Synchronization Control software is custom software created for this project by National Instruments.

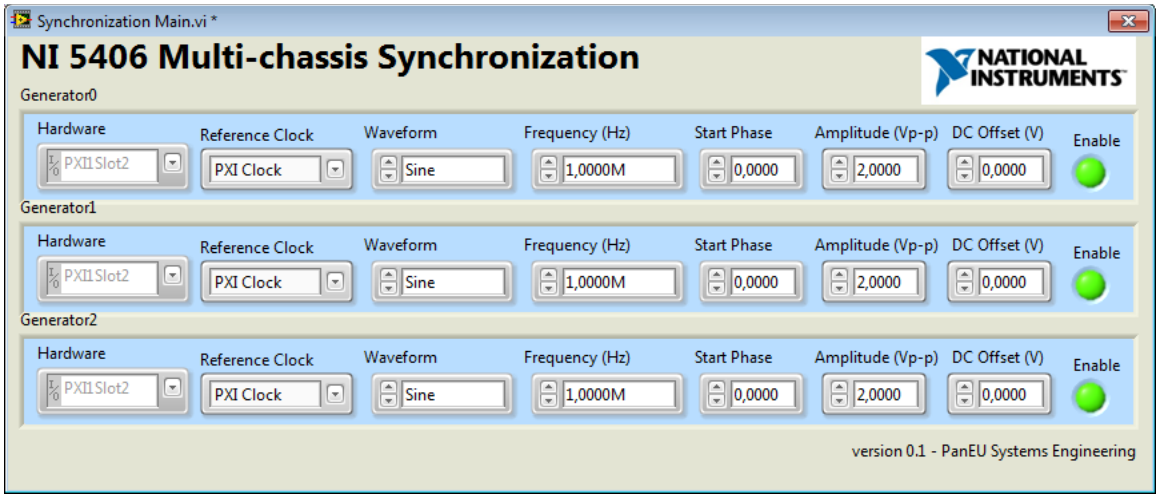


Figure 3-10. Function Generator Control Software

3.1.4 Software development environment

National Instrument's platform includes a programming environment based on LabView graphical system design.

3.1.4.1 NI LabVIEW Graphical System Design

LabVIEW software is used for measurement or control system, and constitutes the main element of the NI design platform. LabView integrates all the tools that are needed to build applications and offers an integration environment for developing the demonstrators. The Figure 3-11 illustrates the basic principles of the platforms composed by a graphical user front panel and a block diagram structure where the codes can be developed.

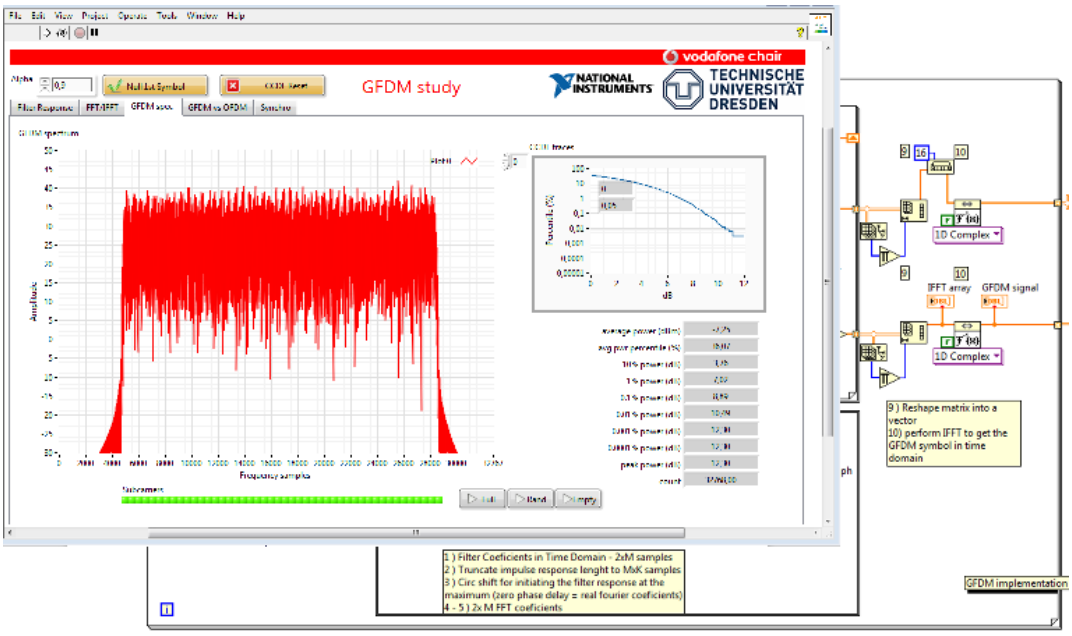


Figure 3-11. LabVIEW Design (GFDM simulator - TUD)

3.1.4.2 LabVIEW FPGA module

NI LabVIEW and the LabVIEW FPGA Module deliver graphical development for FPGA chips on NI reconfigurable I/O (RIO) hardware targets. With the LabVIEW FPGA Module, it is possible to develop FPGA VIs on a host computer running Windows, and LabVIEW compiles and implements the code in hardware. This allows the creation of embedded FPGA VIs that combine direct access to I/O with user-defined LabVIEW logic to define custom hardware for applications such as digital protocol communication, hardware-in-the-loop simulation, and control prototyping (Figure 3-12).

While the LabVIEW FPGA Module contains many built-in signal processing routines, it also integrates existing hardware description language (HDL) code as well as third-party IP including Xilinx CORE Generator functions. In addition, LabVIEW FPGA integrates with both Mentor Graphics ModelSim and included Xilinx ISim tools for cycle-accurate simulation of logic.

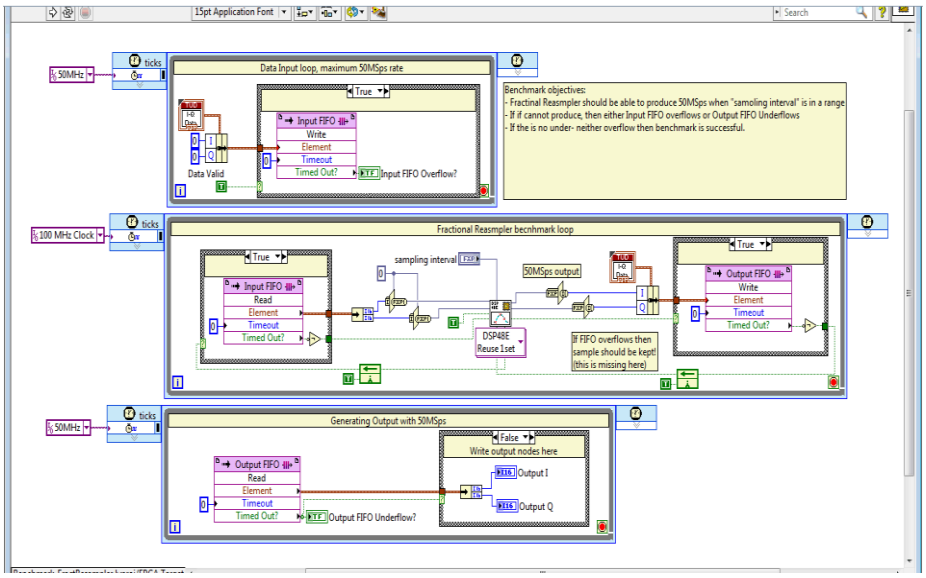


Figure 3-12. LabVIEW FPGA Design (fractional re-sampler used at TUD demo)

3.1.4.3 *Toolkits and Add-ons (used in 5GNOW demonstrator)*

The *NI Modulation Toolkit* extends the built-in analysis capability of NI LabVIEW and LabWindows/CVI software with functions and tools for signal generation, analysis, visualization, and processing of standard and custom digital and analog modulation formats. With this toolkit, you can rapidly develop custom applications for research, design, characterization, validation, and test of communications systems and components that modulate or demodulate signals. The Modulation Toolkit applications include digital modulation formats (AM, FM, PM, ASK, FSK, MSK, GMSK, PSK, QPSK, PAM, and QAM) that are the foundation of many digital communication standards found in 802.11a/b/g/n, ZigBee (802.15.4), WiMAX (802.16), RFID, satellite communications, and commercial broadcast among others.

The *NI LabVIEW Digital Filter Design Toolkit* extends LabVIEW with functions and interactive tools for the design, analysis, and implementation of digital filters. New digital filter users can explore classical designs with the built-in interactive design tools, while experienced users can find a breadth of algorithms, filter topologies, and analysis tools for both fixed- and floating-point digital filters. For fixed-point filters, it is possible to model quantization effects, optimize numeric representation/topology, and deploy the design on a digital signal processor or FPGA using automatically generated ANSI C or LabVIEW FPGA code.

The *Advanced Signal Processing Toolkit* is a suite of software tools, example programs, and utilities for time-frequency analysis, time-series analysis, and wavelets.

DSP Design Library is a toolset which is installed with NI 5791 driver (FlexRIO Adapter Module Support driver). This toolset contains functions (called as "SubVIs") for LabVIEW FPGA and provides very effective way for programming signal processing functionalities, like digital up- and down-conversion, fractional re-sampling, digital offset, gain and wideband equalization.

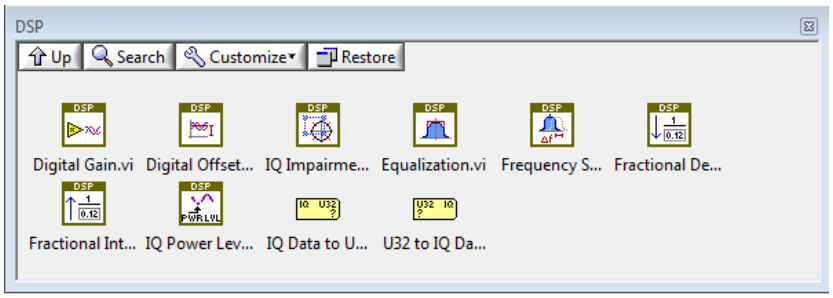


Figure 3-13. DSP Design Library Functions

LabVIEW FPGA RF Communications Library is function collection of FPGA VIs for developing communication applications. This contains encoder, decoders, modulation/demodulation VIs, basic measurements and utilities (ni.com/labs -> LabVIEW FPGA RF Communication Library).

3.1.5 NI USRP-2942R

The NI USRP (Universal Software Radio Peripheral) RIO devices provide a flexible software-defined radio platform which combines a state-of-the dual RF transceiver with a user programmable high performance Xilinx Kintex-7-FPGA (410T) in a half-1U rack-mountable form factor. Different RF frequency options are available. The RF transceiver of the USRP-2942R (selected for the real-time demonstrator described in section 5.4) provides tunable RF center frequencies between 400MHz and 4.4GHz with a per channel real-time bandwidth of 40MHz. The USRP RIO devices can be connected

via a PCI Express connection with either a standard PC, a laptop, or a NI PXI chassis hosting a NI PXI embedded controller. National Instruments LabVIEW graphical programming environment is used for implementing, integrating, and controlling the demonstrator application on the NI USRP RIO devices. For further details it is referred to [NI14a], [NI14b].

Figure 3-14 NI USRP-2942R

3.1.6 NI VST

NI vector signal transceivers (VSTs) combine a vector signal analyser and vector signal generator with a user-programmable FPGA for real-time signal processing and control. Built on the NI LabVIEW reconfigurable I/O (RIO) architecture, it delivers programming flexibility and cutting-edge RF hardware to meet the most challenging RF applications.

3-15: NI PXIe-564xR Vector Signal Transceiver

NI VST as channel emulator

Channel Emulator for joint simulation is implemented on vector signal transceiver (NI VST) [NI14c] which emulates the over-the-air (OTA) channel for a wireless communication link. The wireless

channel emulator is implemented using LabVIEW Desktop and LabVIEW FPGA 2012 and is based on the VST streaming sample project. By combining floating point host code and fixed point FPGA code, the channel emulator provides flexible channel profiles and models that can be easily added and/or modified. We provide two custom channel profiles which are deterministic and stochastic with multiple input multiple output (MIMO) configurations. The channel emulator example can be run as is, or extended to more sophisticated ones by users, since the entire source code is written using LabVIEW.

The NI channel emulator comes ready to run with a pre-compiled LabVIEW FPGA bit file, but all the source code for both the host and FPGA are provided in the project as well. In order to successfully see the effect of the NI Channel Emulator example, the user would need to setup an RF signal source to provide the transmitted RF signal, and a RF signal analyser to see the effect of the fading channel on your signal.

The channel emulator provides two channel fading profiles which are "Deterministic" and "Stochastic" fading.

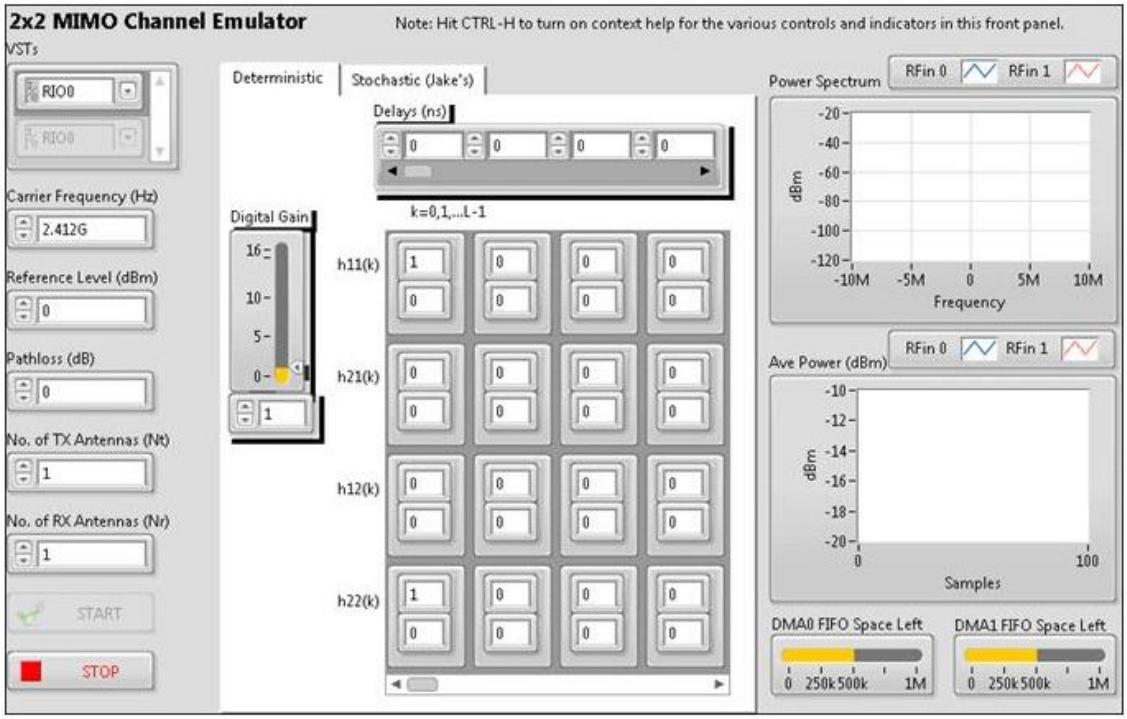
Deterministic fading profile

The *Custom-Deterministic* fading profile allows the user to set the power delay profile (PDP) on the fly. By changing the delays and relative power settings, different frequency selective fading channel can be emulated. In this profile, the channel coefficients are time invariant, i.e. fixed until changed.

Stochastic (Jake's) fading profile

The *Stochastic* fading profile is similar with the *Custom-Deterministic* fading profile, but the channel coefficients are time varying. It generates random channel coefficients that have the statistical properties of the user-set PDP and Doppler spread.

The figure below shows the front panel for Deterministic and Stochastic modes.



3-16: Software Front Panel of Channel Emulator

2x2 Offline Generator software

The described software realizes a 2-channels wireless transmitter which allows to continuously generating different periodic signals (up to 10.4 seconds length) with variable output power, frequency and time delay.

Each channel transmits its own periodic signals which is available in a user selectable file and can be generated with specific output power, frequency and time delay.

Hardware setup is same with 5GNOW hardware platform. 2-channel generation requires the following setup:

1) NI PXIe-1082 8-slots (3U) PXI Express chassis (1x)
2) NI PXIe-8133 2GHz Quad-Core PXI Express controller (1x)
3) NI PXIe-7965R NI FlexRIO FPGA Module for PXI Express (2x)
4) NI 5791 RF Transceiver modules for NI FlexRIO (2x : 1xMaster + 1xSlave)

Required cables connections for Phase-coherent generation:

- SMA to SMA cable to connect Master device (NI 5791) LO Out to Slave device LO In (1x)
- SMA to SMA cable to connect Master (NI 5791) CLK Out to Slave CLK In (1x)

3-17: Hardware configuration of the entire PXI 2-channel wireless trasmitter system

Software is provided and available as executable and full LabVIEW source. FPGA is pre-compiled for PXIe-7965R FlexRIO target; other target may require re-compilation.

Graphical user interface

The main graphical user interface will appear as soon as the executable TX.exe or the [HOST] Main_TX.vi has been started.

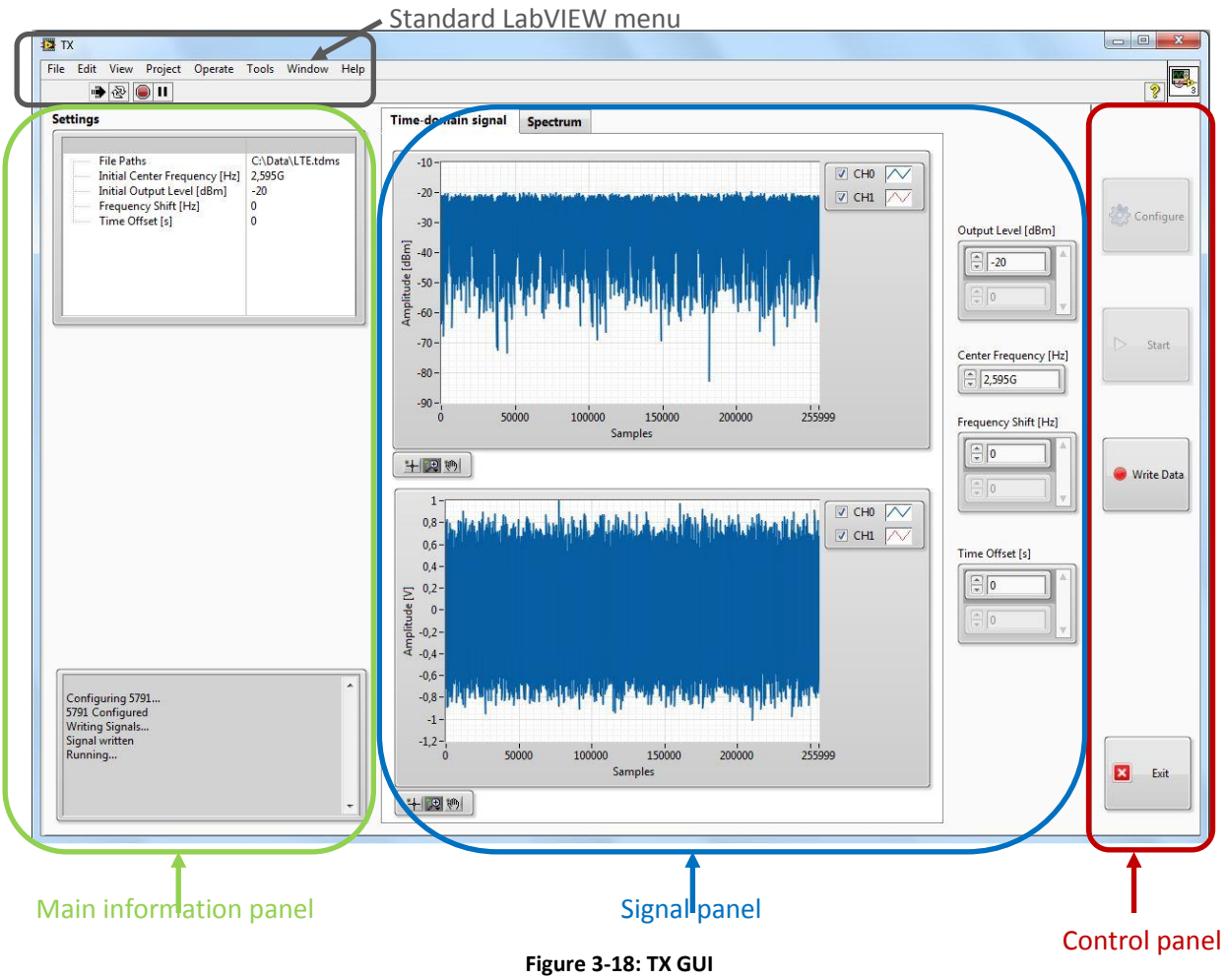


Figure 3-18: TX GUI

As can be seen the GUI is divided into 3 main parts:

1. The main information panel
   - Provides information about basic configuration settings
   - Provides information like ADC overflow
   - Provides detailed system log messages (and error messages)
2. The signal panel
   - Provides several time- and frequency-domain signal plots
   - Supports fine-tuning of the reference level, center frequency, frequency shifts and time offsets
3. The control panel
   - Used for controlling the transmitter application in general

Signal transmission

When the **"Start"** button is clicked, the hardware will be configured using the confirmed parameter settings. As soon as the configuration is done, data will be read from the file and send to the FlexRIOs to be generated and one signal snapshot (of length ***Snapshot Length***) will be sent to the GUI.
By means of these signal plots the following can be checked at this state of operation:

- Is the intended signal really transmitted?
- Is the ADC excitation OK in general? (Full ADC excitation range goes from amplitude -1 … 1.)
- Is the selected center frequency OK, i.e. is the expected signal spectrum centered around zero?

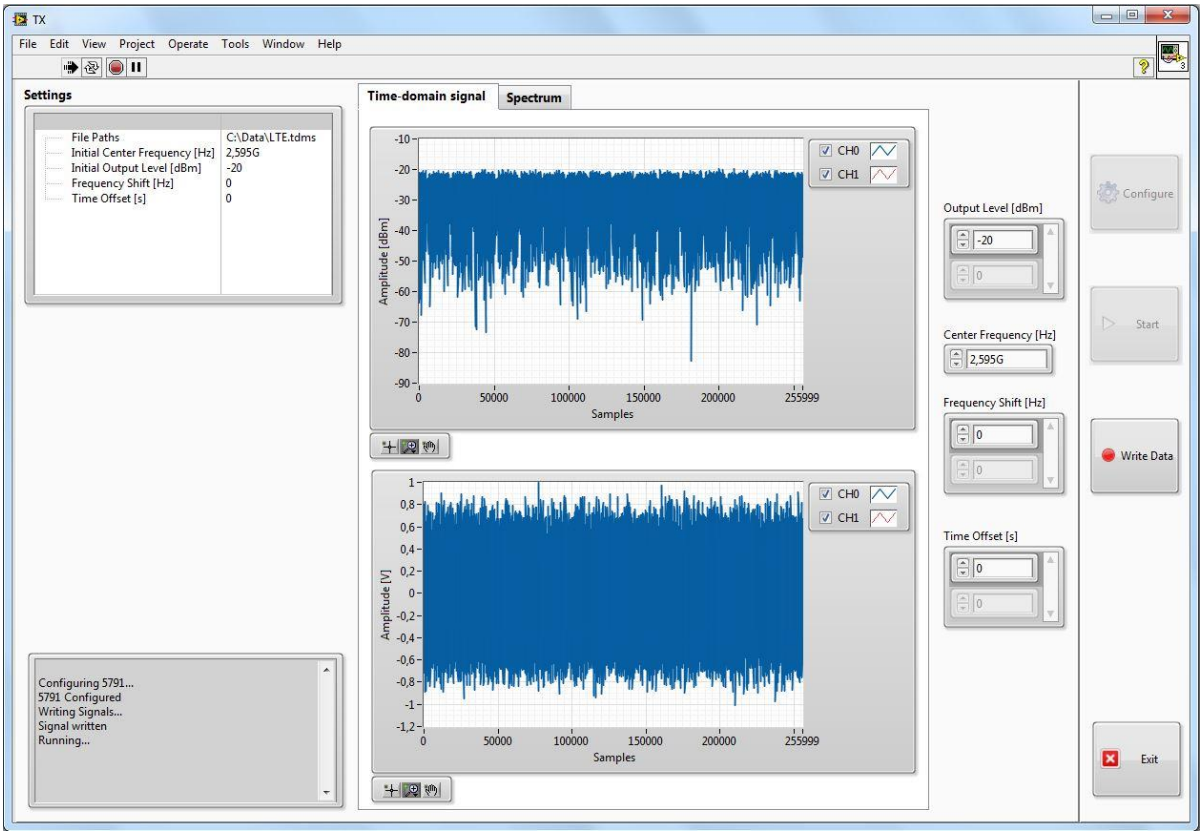


Figure 3-19: GUI with time-domain plots

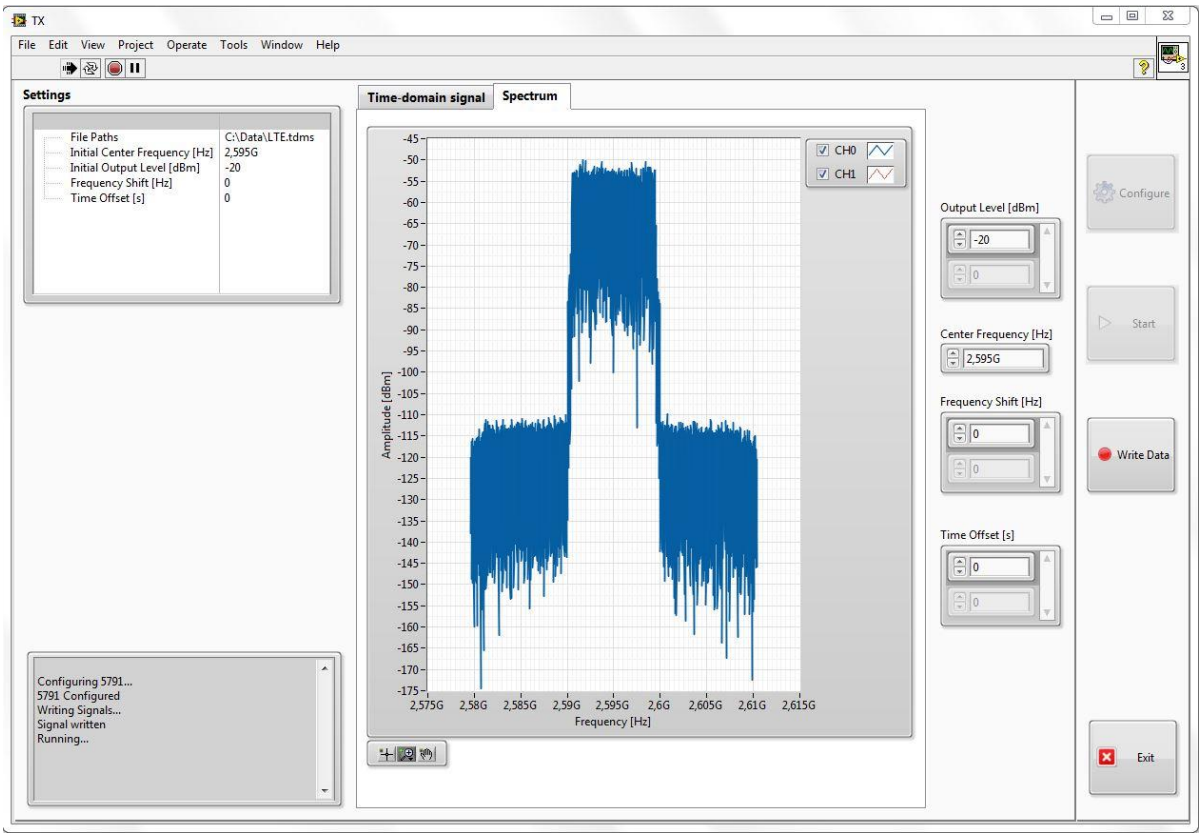


Figure 3-20: GUI with spectrum plot

By means of the controls **"Output Level"**, **"Center Frequency", "Frequency Shift"** and **"Time Offset"** on the signal panel the transmitter gain as well as the center frequency and the time offset between signals can be fine-tuned now. After every change of one of these parameters the signal plots will be automatically updated.

When the **"Write Data"** button is clicked the configured files will be downloaded again to the FlexRIOs.

File formats

The I/Q data of the signals to transmit has to be available as TDMS or MAT file.

The National Instruments TDMS (Technical Data Management Solution) file format is a structured binary file format with some descriptive information. By both file formats I and Q data has to be stored in 2 separated channels, first I and then Q.

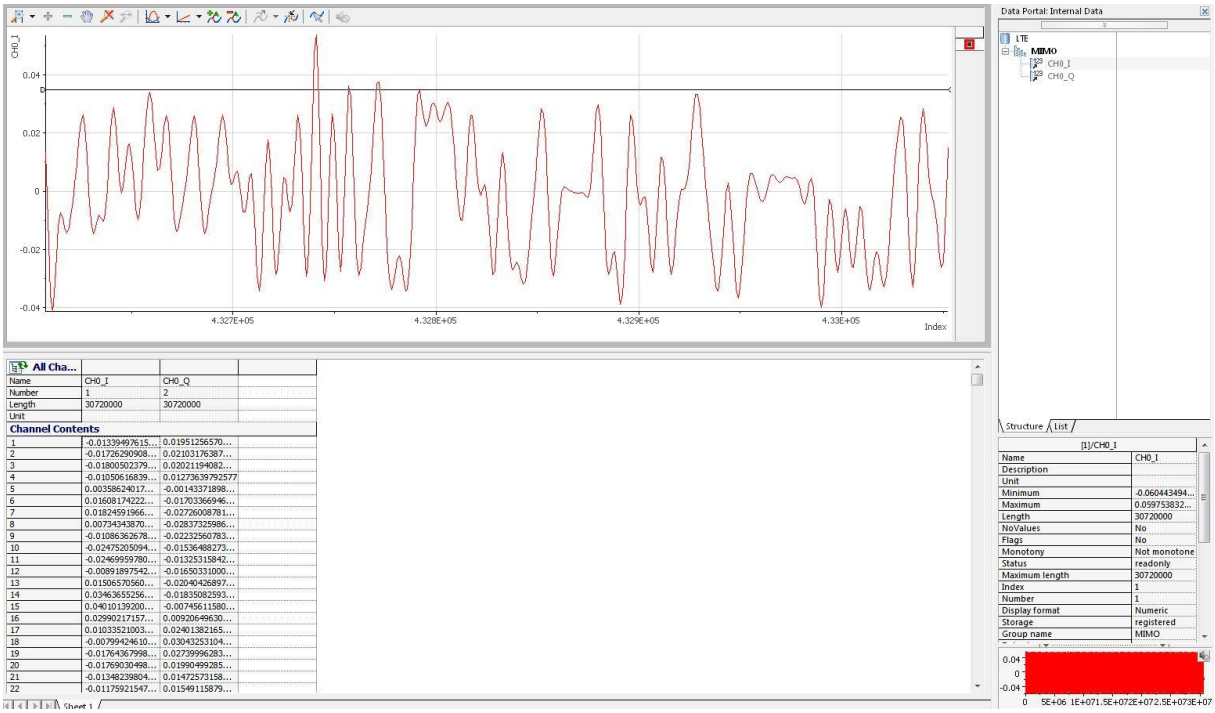


Figure 3-21: TDMS transmitter data file – DIAdem

3.2 CEA-Leti base band platform

The Leti platform for 5GNOW project demonstration is composed of 2 different boards developed by CEA-Leti. The main board is used for Baseband processing, and a specific daughter board is used for Intermediate Frequency (IF) interfacing with NI PXIe chassis. These 2 boards are duplicated for Transmitter and Receiver. The material is identical for Transmitter and Receiver, only their programming is different between TX and RX sides. For the final UL demonstration, two transmitters (UE) and one receiver (BS) are considered.

3.2.1 Architecture of 5GNOW FBMC Demonstrator

On 5GNOW FBMC demonstrator, baseband processing is done on CEA-Leti boards whereas radio transmission at 2.7 GHz is done using NI equipment: PXI-5610 and PXI-5600. The interface between CEA-Leti's equipment and NI's equipment is done with only one analog signal at an intermediate frequency of 25 MHz at the transmitter and 15 MHz at the receiver (see details in section 3.2.5).

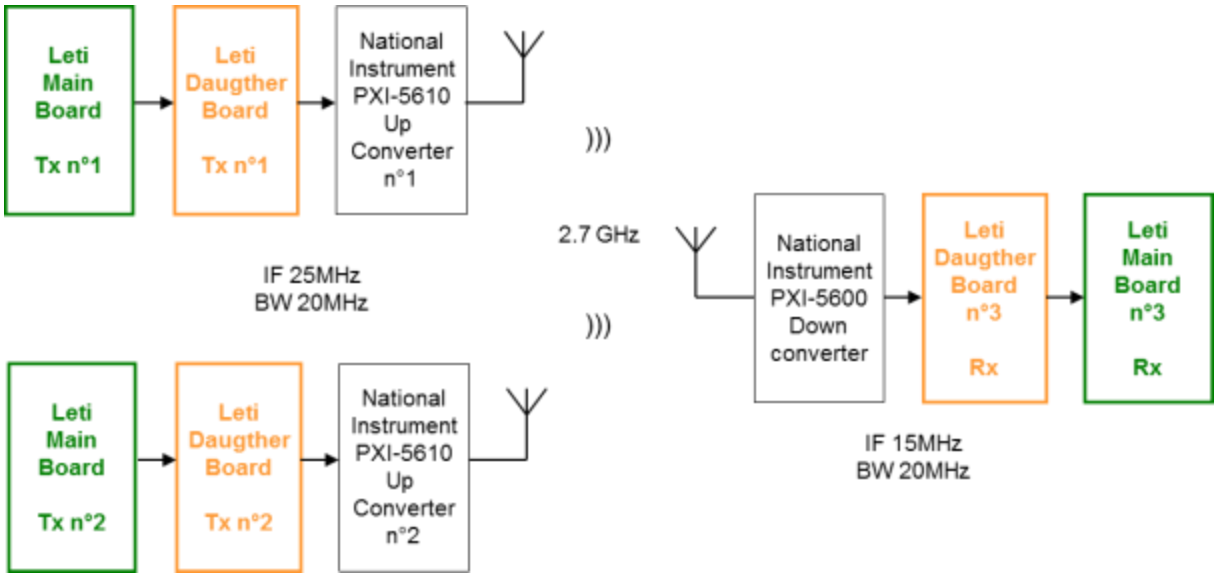


Figure 3-22. 5GNOW FBMC demonstratror

3.2.2 Main Baseband board

The main Baseband board has a reduced size (160x75mm) whereas it has great calculation possibilities. Indeed, its main components are a Kintex7-325T Xilinx FPGA, a Cortex-A8 ARM microprocessor associated with a TMS320C64 DSP in DM3730 component, with many interfaces possibilities.

3.2.2.1 Main components

The main components of the Baseband board are:

- 1 FPGA Xilinx XC7K325T-1FFG676C (326080 Logic cells / 840 DSP (25x18 multiplier) / 445 Blocks RAM 36Kb)
- 1 ARM microcontroller DM3730CBP100 (cortex A-8 at 1GHz + DSP TMS320C64x)
- 1 package on package memory module MT29C4G48MAZAPAKQ-5 IT (= 4 Gbits Nand Flash + 2 Gbits LPDDR SDRAM)
- 1 TPS65950 integrated power management (DC/DC converters, battery charger, usb OTG interface, audio CODEC…)
- 2 dual ADC AD9643 14 bits / 250 MHz
- 1 quad DAC AD9148 16 bits / 1 GHz (with 3 interpolators, NCO and integrated digital mixer)
- 1 microSD card (compact flash) for ARM programming
- External interfaces:
    - 2 Samtec QSE-020 connectors for daughter board plug-in
    - 2 Picoblade Connectors (12 pins) towards a black/white camera and a color camera
    - 1 miniHDMI Connector (19 pins) towards an infrared camera
    - 1 USB interface High-speed OTG
    - 1 Ethernet interface 10/100 Mbps
    - 1 dual RS232 Transceiver MAX3380E
    - 1 WLAN 802.11 Bluetooth interface using a TiWi-R2 module
    - 2 Jack Audio connectors connected to the onboard audio CODEC (TPS65950)
    - 1 Samtec SFMC-117 connector for interface to a LeopardBoard (camera)

- 1 HDMI connector connected to the onboard graphics controller TFP410 (video HD output)

3.2.2.2 Functional block diagram

The main baseband processing is done in the Xilinx FPGA X7K-325T. The DM3730 digital media processor makes some other calculations in Linux environment and manages the interfaces with the external world.
At the transmitter side, the conversion from baseband signals to an intermediate frequency signal is done inside the AD9148 DAC. At the receiver side, the dual conversion (IF to baseband) is done in the FPGA.

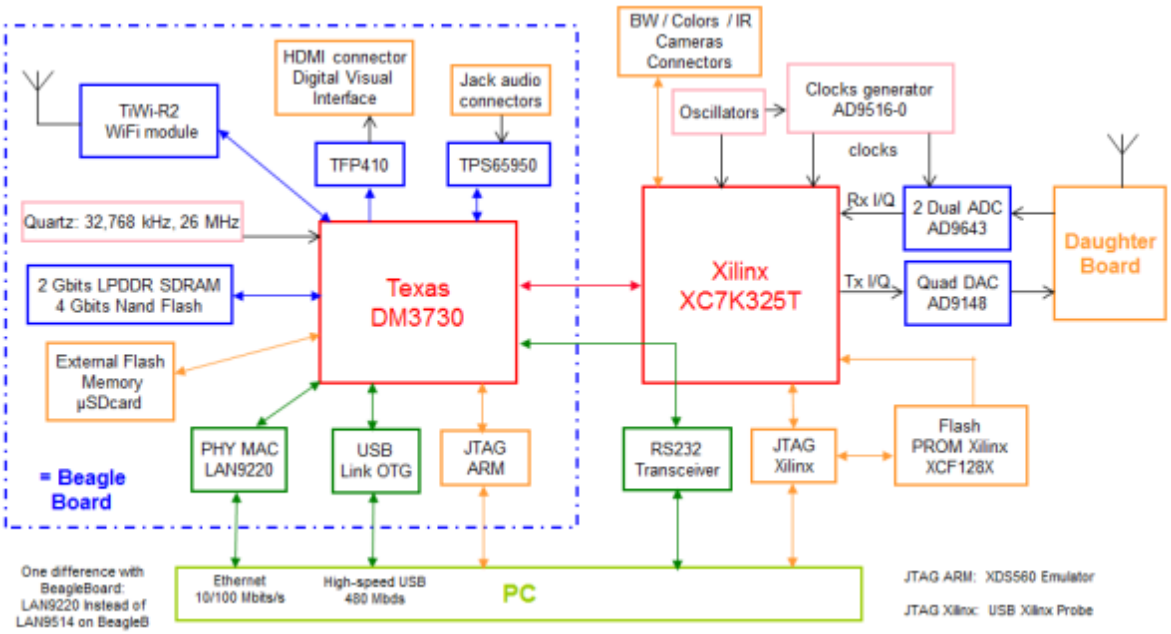


Figure 3-23. Main baseband board architecture

Figure 3-24. CEA-Leti's main board

3.2.3 Daughter board

To solve the interconnection problems between CEA-Leti and National Instruments materials, a specific daughter board has been developed by CEA for the 5GNOW project. This daughter board is plugged on the main board and enables to have the intermediate frequency signals on SMA connectors, directly compatible with PXIe-5600 and PXIe-5610 materials.

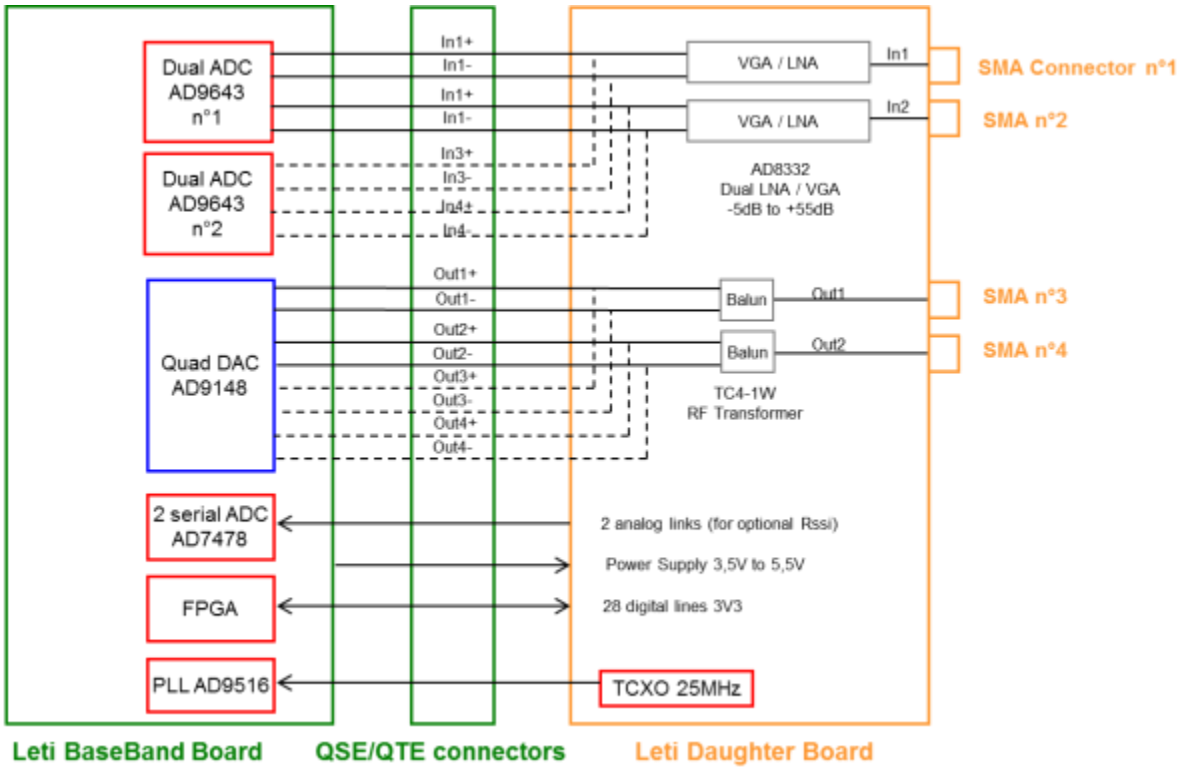


Figure 3-25. Interfaces between main board and daughter board

These two CEA-Leti boards can be inserted in a small 160x78x43 mm aluminium box, including also their Li-ion cell for several hours of battery life.

Figure 3-26. Box for digital base band board

3.2.4 FBMC baseband transceiver implementation architecture

5GNOW TRX baseband transceiver is implemented on an architecture based on a Xilinx Kintex 7 FPGA and an OMAP ARM Cortex. The transceiver physical layer implementation developed in WP5 has been implemented on the FPGA. A general overview of the main modules composing the physical layer architecture is given in Figure 3-27.

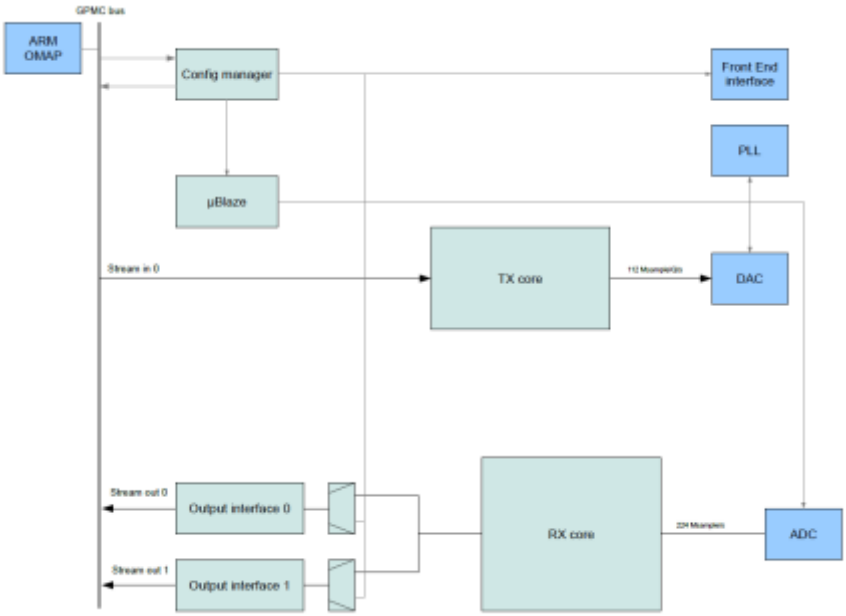


Figure 3-27. Top level architecture for 5GNOW demonstrator

The overall architecture of the baseband transceiver is composed of the following elements:

- ARM OMAP: The main controller of the CEA-Leti's baseband board. A Linux operating system based on open embedded Angström [Ang12] is running on the ARM Cortex A8. The embedded Linux distribution, a Debian version, has been adapted to the peripherals available on the board. Most standard operations may be performed on the ARM as if performed on standard personal computers.
- The FPGA-ARM Interfaces allow for communication between the ARM and the digital transceiver core (i.e.: the FPGA)
- The digital core of the transmitter and the receiver where the implementation design of the FBMC transmitter and receiver is realized.
- The RF interface that includes analog-to-digital conversion, digital-to-analog conversion and control interface to the daughter board.

The ARM Cortex A8 can be used for implementation of software components. Although out of the scope of this document, sophisticated MAC could be implemented on the ARM and constitutes a standalone MAC/PHY combination. An interface between the ARM Cortex A8 and the FPGA has been developed. This interface allows for simple and straightforward software communication with the transceiver. The interface is using the General Purpose Memory Controller (GPMC) of the ARM Cortex A8 in a synchronous mode to transfer data to the FPGA [TI10]. The following strategy has been followed: the FPGA design contains a set of FIFO to transfer data and control from the ARM to the FPGA. The following FIFOs have been considered:

- A Configuration FIFO
- An Input Stream FIFO
- An Output Stream FIFO

Each FIFO is seen as an address for the GPMC controller of the ARM. Input Stream FIFO is "write only", while output stream FIFO is "read only". Read and write to the configuration FIFO is done via different addresses (a read and a write address). A C-library has been developed to access to the different interfaces of the FPGA design.

Figure 3-28 depicts the high level architecture of the demonstrator. Green boxes components are implemented on ARM while blue box components are mapped into the FPGA. The input/output of

the demonstrator are IP streams. It should be mentioned that performance statistics can be easily computed by analysing the checksum attached to each packets.

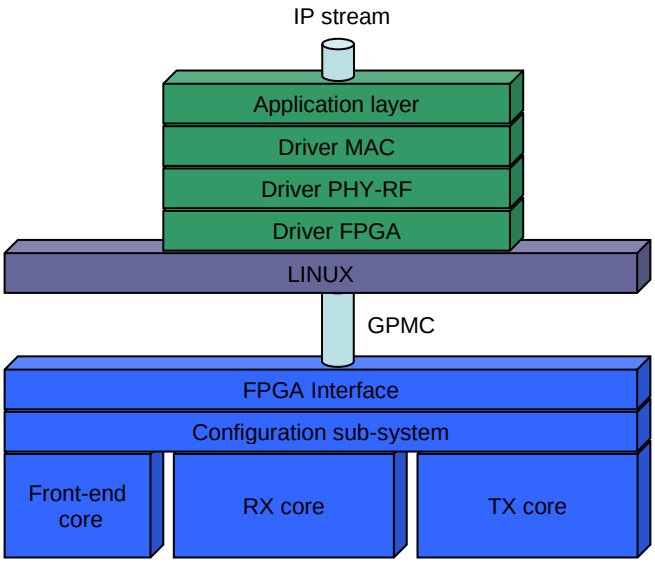


Figure 3-28. High level architecture of the FBMC demonstrator

3.2.5 RF Up-conversion and Down-conversion

As it is mentioned in section 3.2.1 and as can be seen on Figure 3-29 the baseband board is connected to NI RF up-converter and down-converter to be able to extend operating frequency range up to 2.7GHz.

3.2.5.1 IF interfacing with NI PXI Up/Down-converter

NI PXI-5600 (Down-converter) and PXI-5610 (Up-converter) has SMA single ended connectors for interfacing on intermediate frequency analogue signals. Intermediate frequency is 25MHz on PXI-5600 and 15MHz on PXI-5610.

Furthermore these devices can accept external reference clocks and can be synchronized to each-other in order to operating totally on the same carrier frequencies. Reference clock also can be exported on both devices.

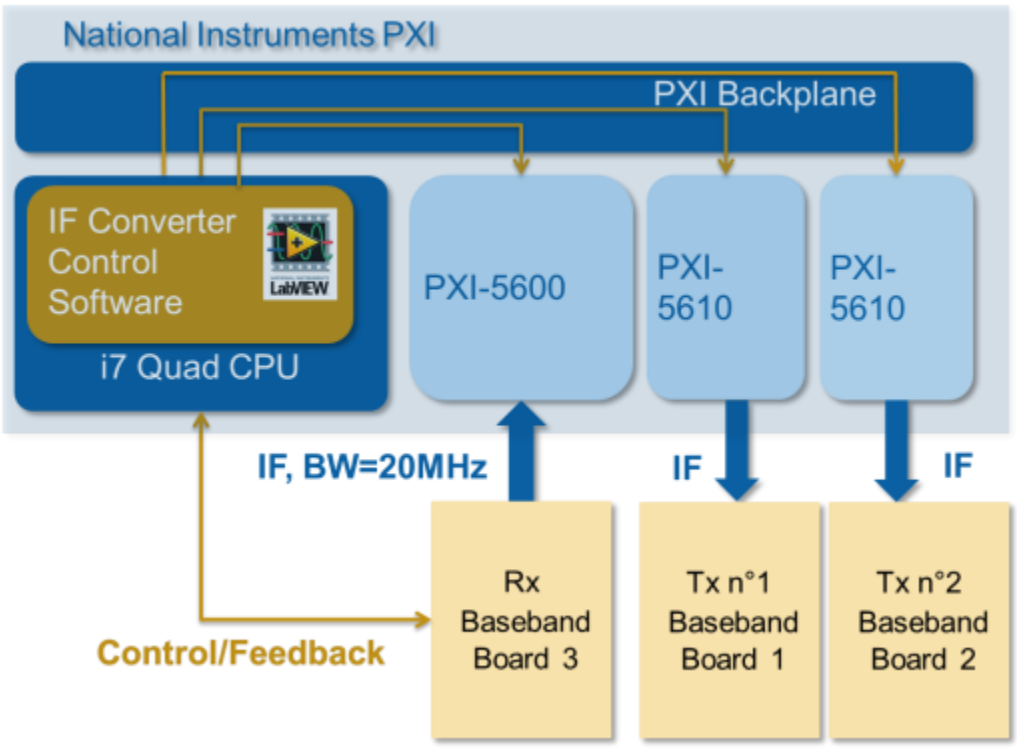


Figure 3-29. Connections between Baseband boards and NI RF modules

NI PXI devices require software control to set the desired carrier frequency, IF bandwidth, RF-IF attenuators and amplifiers (reference level on down-converter and output gain on up-converter), reference clock source, etc.

These parameters can be set from software which runs on the host computer of the PXI system. The software can also have external connections and could communicate with the Baseband Board on common interfaces like USB, serial or Ethernet.

At the moment the control software has a Graphical User Interface (GUI) and parameters can be set manually (Figure 3-30).
Software is a standalone executable which does not require programming. It was created and compiled with LabVIEW, therefore it requires LabVIEW Run-Time Engine (2012 version) for executing.

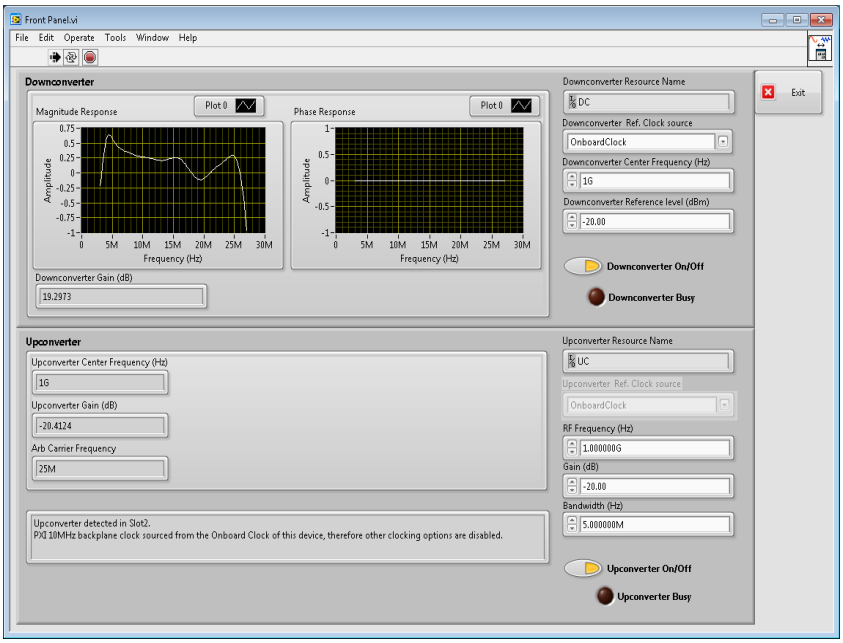


Figure 3-30. Contol software Front Panel (NI LabVIEW)

Figure 3-31. PXI 2.7GHz up- and downconverter with NI 5600 and NI 5610

The NI PXI-5600 is a modular, broadband down-converter in a compact, 3U PXI package. The PXI-5600 features a wide real-time bandwidth and a highly stable time-base, accurate to within ±50 ppb. It provides integration with modular digitizers for RF analysis applications.

- 9 kHz to 2.7 GHz
- 20 MHz real-time bandwidth
- +30 dBm full scale input range
- <-135 dBm/Hz average density
- 80 dB spurious-free dynamic range
- High-stability OCXO timebase

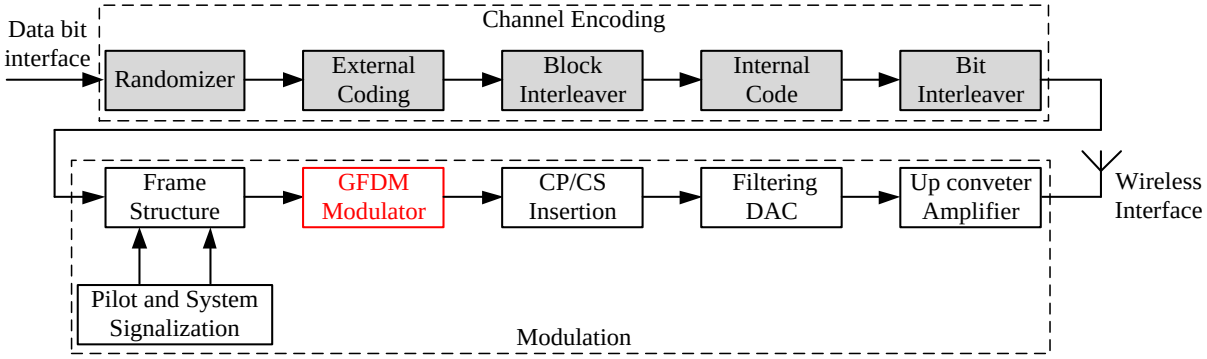
4 Final implementation of transceiver algorithms and control functionality in the 5GNOW PoC

4.1 GFDM transceiver

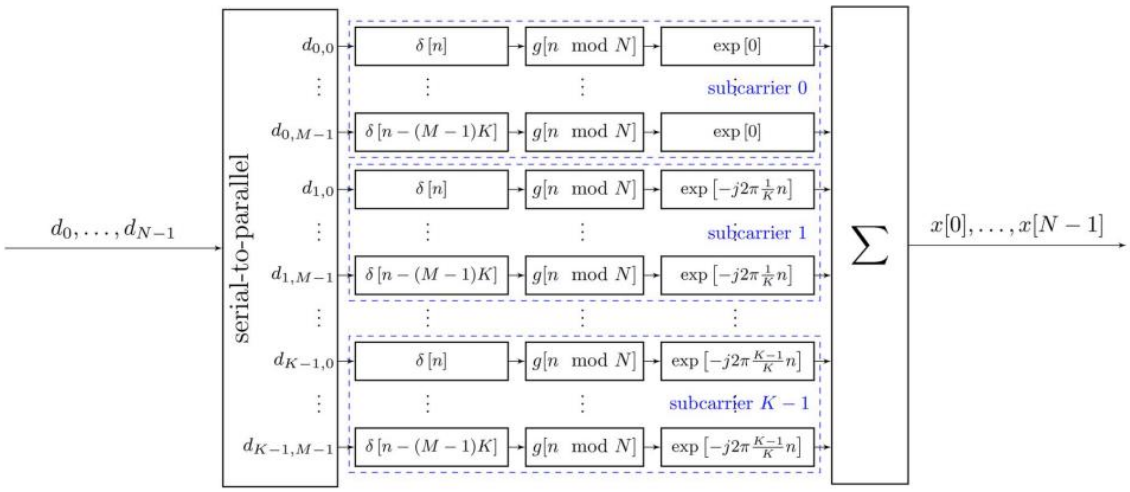
GFDM is a filtered multicarrier modulation scheme that can transmit sequences of circularly pulse shaped symbols per subcarrier with or without cyclic prefix extension. GFDM can perform OFDM (Orthogonal Frequency Division Multiplexing) as a special case when configured to transmit one square pulse shaped symbol per subcarrier. Its flexibility to provide localized spectrum properties has the potential to alleviate issues of synchronization and carrier aggregation in future wireless communication systems.

Figure 4-1 (a) presents the simplified block diagram of the GFDM transmitter. The block diagram is divided in two main macro blocks: Channel Encoding and Modulation. The main objective of the channel encoding is to protect the information against the channel impairments while modulation represents the data bits using an appropriate non-orthogonal waveform. Although all blocks in the diagram are required to achieve reliable wireless communication, the focus of this project is the development of the Modulation blocks, which means that the implementation of dark block is out of the scope of this project. The Channel Encoding blocks are presented here to demonstrate a possible complete communication chain using GFDM as waveform.

The data sequence is first applied to a Randomizer that is responsible for uniformly distribute the energy of the bit sequence in the entire available bandwidth by multiplying the incoming bits with a pseudo-noise bit sequence. The randomized data is applied to the external channel encoder, which adds redundancy information to protect the data. Different codes can be used here, according to the application scenario and channel conditions. The encoded data is block interleaved to avoid burst block errors in the receiver side. An internal code is applied in to the block interleaved sequence aiming to increase robustness against the channel impairments. After the second encoding process, the data is bit interleaved to avoid burst bit errors. The Frame Structure block organizes the data and maps the information bits in QAM symbols. Also, this block adds the systems information, pilot and synchronization signals. GFDM modulator employs M sub-symbols per sub-carriers and K different subcarriers to transmit MK QAM symbols. More details about the implementation of the GFDM modulator block, Figure 4-1 (b), are presented in sections 4.1.1 and 4.1.2. CP and CS can be added to the GFDM signal to increase robustness against multipath channel and to relax the synchronization requirements in RACH scenarios. After filtering and digital-to-analog conversion, the signal is up-converted to the channel frequency, amplified and delivered to the transmit antenna.



(a)



(b)

Figure 4-1 (a) Simplified block diagram of the GFDM transmitter. (b) GFDM modulator block diagram

Figure 4-2 depicts the simplified block diagram of the receiver. Again, the block diagram is divided in two parts, where the first consists on the Demodulation process and the second part is the Channel Decoding process. It is important to highlight that only the blocks within the demodulation will be implemented in this project and the dark blocks are out of the scope of this project.

The received signal is down converted, amplified and sampled before being applied to the Synchronization block, where the time and frequency alignment is performed, when necessary. The Synchronization block indicates the beginning and end of the GFDM symbol, allowing for the CP and/or CS to be properly removed. The Synchronization block also delivers information for the Channel Estimation block, where the estimated channel frequency response is obtained. The signal is equalized and delivered to the GFDM receiver. Different approaches can be used to recover the information from the equalized GFDM symbol and more details about this procedure are available in section 4.1.3. The received symbols are de-mapped and the system information is removed from the data stream by deframing. The resultant bit sequence is de-interleaved, spreading eventual error bursts and increasing the performance of the internal decoder. After internal channel decoding, the data sequence is block de-interleaved and external channel decoder aims to remove the remaining errors in the received data sequence. Finally, the receiver randomizer, which is synchronized with the transmit randomizer, multiplies the decoded sequence by the same pseudo-noise sequence, delivering the data recovered information in the data bit interface.

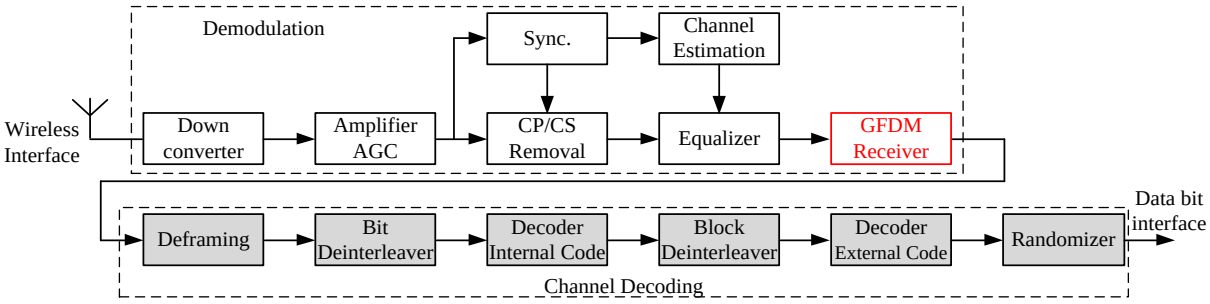


Figure 4-2 Simplified block diagram of the GFDM receiver chain.

In the following results of a proof of concept implementation of the transmitter using a NI PXI software defined radio platform and the LabVIEW FPGA module will be detailed.

4.1.1 Low complex TX model

The GFDM multicarrier signal is built with K active subcarriers and M active time slots. Each subcarrier is pulse shaped with a transmitter filter and modulated with a specific subcarrier center frequency. Each symbol is sampled $N \geq K$ times leading a total of MN samples per subcarrier, which is necessary in order to satisfy the Nyquist criterion. The transmit data signal is obtained through superposition of the filtered data symbols of all subcarriers and time slots. An important characteristic is that the filter response is cyclic with an interval of MN samples, resulting in an equivalent circular convolution operation. In time domain the number of complex valued multiplications necessary to produce this operation are NKM^2, so, from a hardware perspective, a straightforward implementation of the described model is not suitable for practical values. The solution comes from reformulating the GFDM transmitter in a fashion that is similar to the well-known IFFT/FFT approach that is used in OFDM. Instead of performing pulse shaping in time domain, the circular convolution can be alternatively obtained by a multiplication operation in frequency, supported by a back and forward Fourier transformation.

With this approach, the data up sampling operation in time domain, using zero stuffing between the symbols, turns into a spectrum repetition pattern of the corresponding samples in frequency domain. Thus the result can be equally produced by copying the spectrum of smaller M-point FFT, instead of actually performing arithmetic operations necessary for an NM-point FFT. Also, since the aim of the pulse shaping is to keep out-of-band radiation minimal, the utilized pulse may turn out to be sparse in frequency domain, i.e. many of the coefficients can be zero and thus multiplications do not need to be carried out. In line with the requirements for strong out-of-band attenuation, filter pulse spans only over its immediate neighbours in frequency domain. For instance, the non-negligible coefficients of a Root Raised Cosine pulse with a roll-off factor 0, which is an ideal square filter in frequency with 0% excess bandwidth, implies in the processing of only the Nyquist bandwidth of the subcarriers, represented by M frequency samples. On the other extreme, a roll-off equal to 1 produces 100% excess bandwidth, requiring in this case $2M$ points (2 times spectrum repetition) to be properly represented. Furthermore, the DFT of the modulation carriers corresponds to Dirac impulses in frequency domain and the convolution with it results in a simple position shift of the coefficients. Consequently, the subcarrier up conversion can be implemented by re-aligning the samples in frequency domain. Lastly, the subcarriers are summed up, composing the NM-point spectrum samples of the GFDM signal, which is converted back to time through an IFFT operation.

The operations listed above leads to a low complex GFDM transmitter model. The operations can basically be executed in a pipeline structure that sequentially processes *N* chunks of *M* samples, processing and combining them in a tapped delay line illustrates how a set of 3 subcarriers (labelled as waveforms M1 to M3) can be processed sequentially.

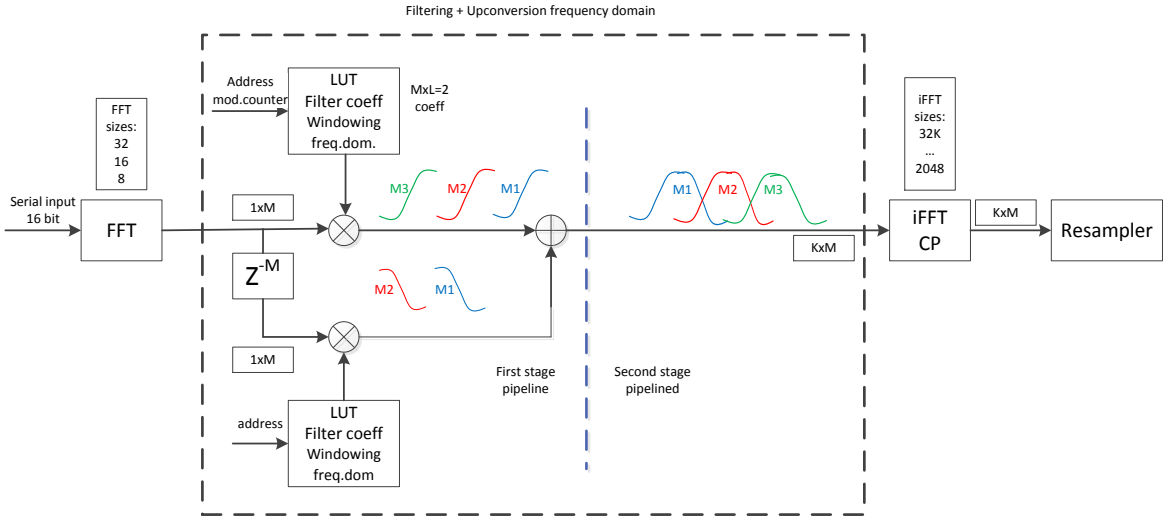


Figure 4-3 GFDM transmitter FPGA pipelined implementation

The M-points spectrum of the subcarriers data is repeated and shaped by the coefficients of the transmitter. The 2-stage pipeline structure performs the filtering process per subcarrier in the frequency domain, by separating the filter into two parts. In the first stage of the pipeline, the current active subcarrier, *k*, is filtered by the first half of the pulse shape, by means of doing an M-point complex multiplication. In parallel the previous $(K\text{-}1)^{th}$ subcarrier is filtered with the second half of the pulse shape. The filter coefficients of the pulse are saved in lookup-tables for both filter halves. Then, both sequences will be added to build the overlapped half spectrum of the k^{th} subcarrier with the $(K\text{-}1)^{th}$ active subcarrier. Non active subcarriers are basically obtained by nulling the data in the input.

The M point FFT needs to be adaptable in length in order to provide a flexible transceiver structure for different scenarios, i.e., machine type communications, low and high data rate communications, multipath channel conditions, etc. By using this structure the output of the adder represents the natural order of the modulated subcarriers in the spectrum. The expected hardware costs for implementing the oversampling, filtering process and up conversion to the subcarrier frequency are 2 parallel structures of *M*-point complex multiplications, *M*-point delay memory and *M*-point complex additions.

Doing this process for *K* subcarriers, at the output of the adder a *KM* point sequence in frequency domain is set up. In the next step this sequence will be transformed into the time domain by an IFFT of *NM* points. The IFFT should be adaptable in length, like the first FFT block.

4.1.2 GFDM Transmitter prototype using NI-PXI-7965

Moving the digital signal processing to the FPGA allows the implementation of a high throughput GFDM stream. For this purpose, different timed loop structures have been employed. Three of them are used for configuring the RF front end and block RAMs.

For the digital baseband processing of the GFDM subcarriers a parallel structure of three timed loops with FIFO data exchange was developed. The input of the GFDM transmitter can either be fed by a random QAM symbol generator or by fixed predefined signals that can be loaded into block RAMs. The coefficients for the frequency domain filter process are also stored in memory blocks and can be easily exchanged by a different set of coefficients via the RT processor over a DMA in the configuration routine of the transmitter. Two instances of the Xilinx FFT core perform an *M*-point FFT (with M=8, 16, 32) and an *N*-point IFFT (with N = 64, 128,…, 32768), respectively. The IFFT core supports run-time configurable transform point size and streaming architecture. A wrapper was required to realize handshaking mechanisms that control the IFFT core activity to avoid FIFO overflows and underflows. This mechanism allows adapting the IFFT throughput on the actual transmitter sample rate while keeping the output FIFOs small. Finally, the NI fractional re-sampler adapts the I&Q sample rate to the DAC sampling frequency of 50MHz.

The transmitter was designed with a backlog mechanism in such a way that no overflows occur in the FIFOs (Figure 4-4). The bottleneck process in the design is the loop that feeds the DAC. Working usually with bandwidths between 20 and 50 MHz, it is possible to continuously generate GFDM blocks up to 32768 samples length.

The acquisition of signals in the FPGA is possible. The hardware resources and the Graphical User Interface (GUI) needed for this implementation are shown in section 5.1.1.

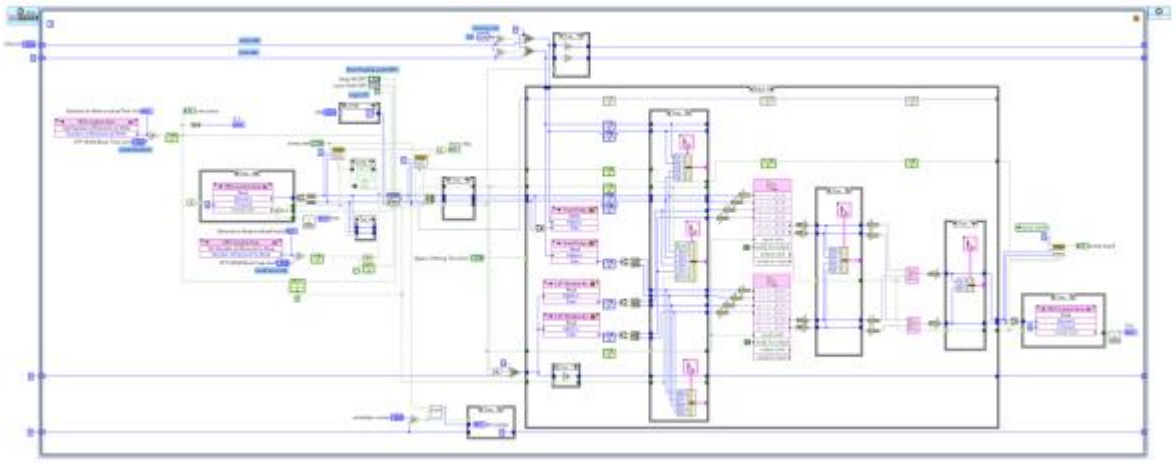


Figure 4-4 Timed Loop IFFT of a GFDM Frame

4.1.3 Low complex RX model

A detailed description of a low complex receiver structure proposed to GFDM can be found in [Gas13]. In the following a brief description of the intended future implementation will be presented.

The approach is similar to the transmitter approach; it is based on based on block diagrams that can implement the main equations that describe a GFDM receiver in a pipeline mode. To better support the block diagram description let us review the equation that produces the GFDM transmitted block **x** given by

$$\mathbf{x} = \mathbf{W}_{MK}^{H} \sum_{k=1}^{K} \mathbf{P}^{(k)} \boldsymbol{\Gamma}_{\mathrm{Tx}}^{(L)} \mathbf{R}^{(L)} \mathbf{W}_{M} \mathbf{d}_{k}$$

which is obtained from *K* column vectors $\mathbf{d}_k$ which represent subcarriers with M symbols each. The process is performed in frequency domain using the DFT matrices $\mathbf{W}_M$ and $\mathbf{W}_{MK}^H$ because this approach allows a low complex implementation of the circular convolution. The matrix $\mathbf{R}^{(L)}$ performs the *L* times repetition of the sub-carriers spectrum, followed by pulse shaping filtering $\mathbf{\Gamma}_{\mathrm{Tx}}^{(L)}$, up-conversion $\mathbf{P}^{(k)}$, and finally the multiplexation of the *K* subcarriers.

The matched filtered version of the receiver follows the structure of the transmitter and for a received signal $\boldsymbol{y} = \boldsymbol{x}$ the subcarrier data can be obtained according to:

$$\hat{\mathbf{d}}_k = \mathbf{W}_M^H \left(\mathbf{R}^{(k)}\right)^{\mathrm{T}} \mathbf{\Gamma}_{\mathrm{Rx}}^{(L)} \left(\mathbf{P}^{(L)}\right)^{\mathrm{T}} \mathbf{W}_{MK} \mathbf{y}$$

Again, the operations are performed in frequency domain and $\left(\mathbf{P}^{(L)}\right)^{\mathrm{T}}$, $\mathbf{\Gamma}_{\mathrm{Rx}}^{(L)}$and $\left(\mathbf{R}^{(k)}\right)^{\mathrm{T}}$represents now down-conversion, filtering and decimation respectively.

The Equations above constitute the basic motivation for the proposition of the block diagram in transmitter and receiver are reproduced side by side to highlight its similarities. Again, it considers *L*=2 so that the pulse shaping process has the flexibility to be represented with a roll-off ranging from 0 to 1. The transmitter receives the *M* input symbols per subcarrier in a sequential sample basis and a domain conversion is obtained by reusing a single DFT component. The spectrum repetition consists basically of a memory block of M positions. The pulse shaping process is performed using a single multiplier with coefficients provided by look up tables (LUT). Each LUT contains half of the transfer function of the filter, denominated here as rise $\mathbf{\Gamma}^{(r)}$ and fall $\mathbf{\Gamma}^{(f)}$ parts. The up-conversion of the pulse shaped subcarriers is naturally obtained with the sequential sum of the samples in transmitter chain and finally converted to time domain by employing a DFT with MK points.

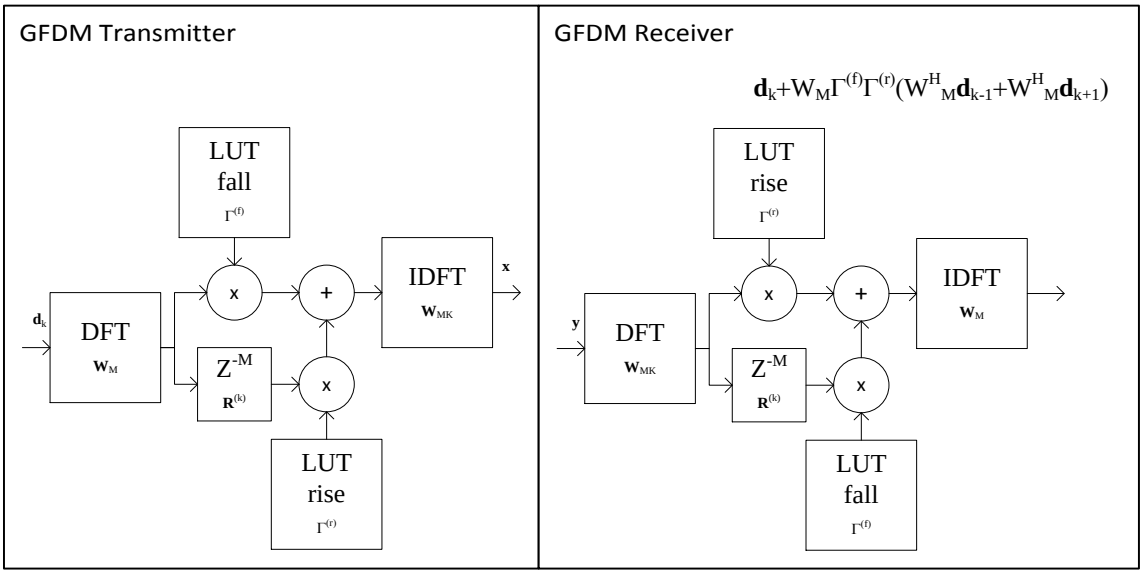


Figure 4-5 GFDM transceiver block diagram

4.1.3.1 Matched filter

The ideal matched filter receiver structure is only slightly different. Considering a perfect synchronization, the received signal is converted to the frequency domain and then processed in small chunks of *M* samples, which after pulse shaped by the receiver filter are decimated by

overlapping its rise and falling spectrum terms. Without considering artifices of Offset QAM in the transmitter, the overlapped regions of the subcarriers will result in inter carrier interference [Gas13]

$$\hat{\mathbf{d}}_k = \mathbf{d}_k + \mathbf{W}_M^H \mathbf{\Gamma}^{(r)} \mathbf{\Gamma}^{(f)} (\mathbf{W}_M \mathbf{d}_{k-1} + \mathbf{W}_M \mathbf{d}_{k-1})$$

The interference can be estimated according to the structure depicted in Figure 4-6. Successive estimations, required in case of high order modulation, are possible with incremental use of hardware resources. Another strategy is the reuse of a single block in a loop operating in a higher clock.

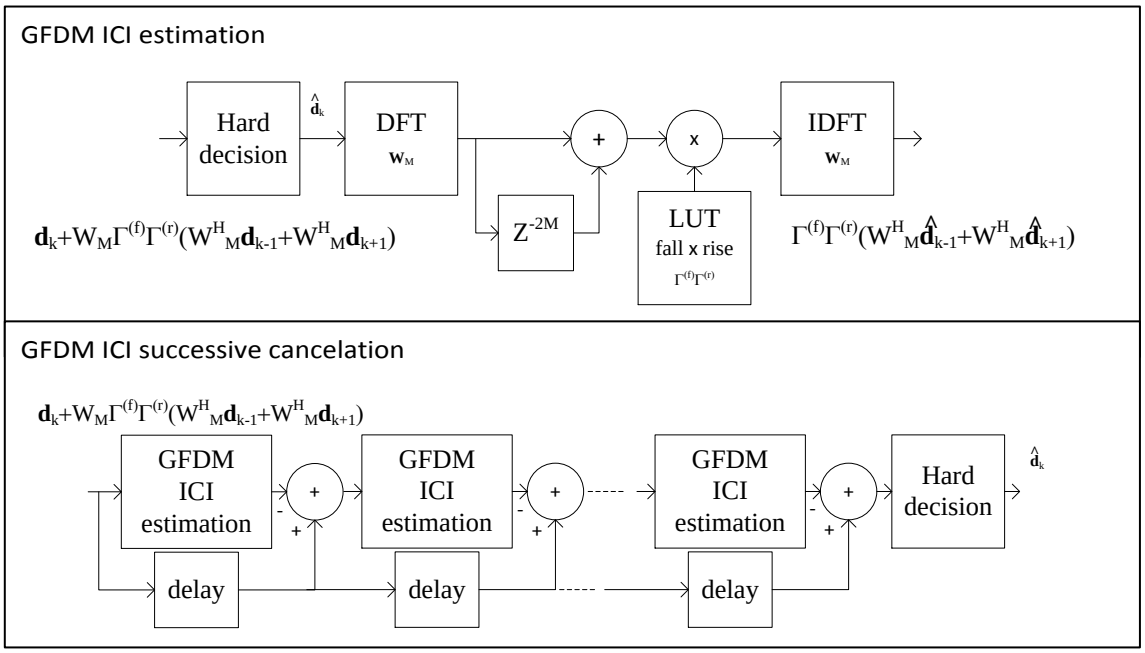


Figure 4-6 GFDM ICI cancelation scheme

4.1.3.2 Zero-Forcing

The ZF receiver inherently removes this interference with a specific receiver filter at the cost of a certain noise enhancement. However, for moderate SNR this noise enhancement is far below the amount of the self-interference of the matched filter.

The main problem with the ZF receiver was the requirement to invert the transmission matrix in order to find the appropriate receiver pulse. Depending on the system size this task is not easily carried out in hardware due to memory and timing constraints. Recent research has found a method to easily calculate the corresponding receiver pulse since it was identified as the canonical dual window to the Gabor frame that is spanned by all time-frequency shifts of the transmit prototype filter. In this setting efficient algorithms for the calculation of the dual Gabor window exist that do not require the inversion of the entire transmission matrix [Sønd12]. In the special case of critical sampling, which occurs in GFDM, these can also be easily implemented in hardware. Figure 4-7 shows the corresponding ZF receive filter for a RC transmit filter with roll-off 0.2.

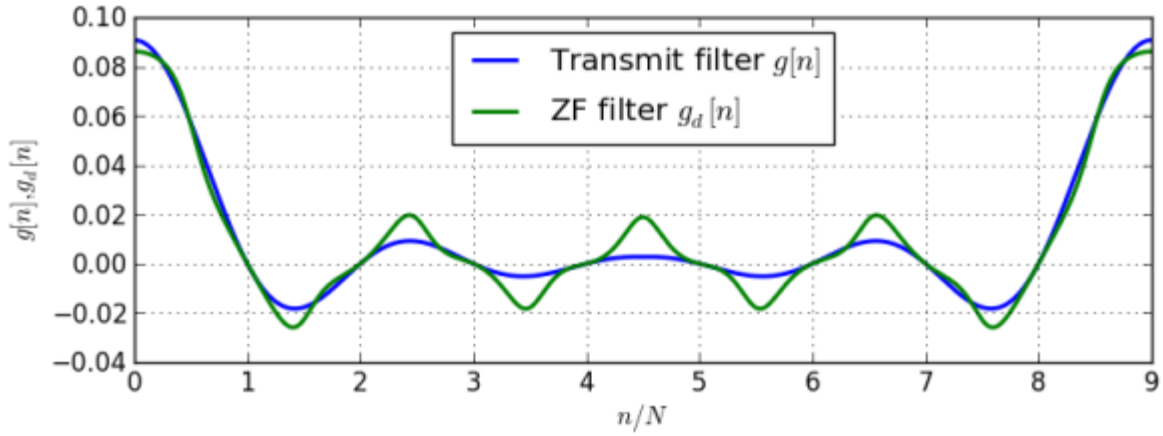


Figure 4-7 Example of transmit and corresponding ZF receiver filter

With the available ZF receive filter the same receiver architecture as for the MF receiver can be employed, but by using a different $\mathbf{\Gamma}_{\mathrm{Rx}}^{(L)}$ that contains the spectrum of the ZF receive filter, as can be seen in Figure 4-8. Furthermore, a larger L needs to be used in the implementation, since the ZF filter is more wide-band. However, this increased complexity here is easily overcome by being able to remove the interference cancellation part from the receiver. The ZF receiver will enable us to use easier channel estimation and synchronization algorithms since no self-interference needs to be taken into account.

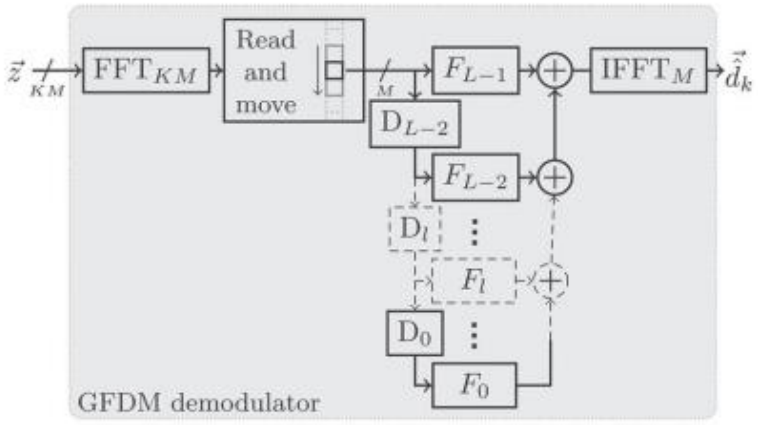


Figure 4-8 Block diagram for receiver for implmenting the ZF filter

4.2 FBMC transceiver

4.2.1 FBMC transmitter

The architecture of the 5GNOW transmitter is depicted in Figure 4-9.

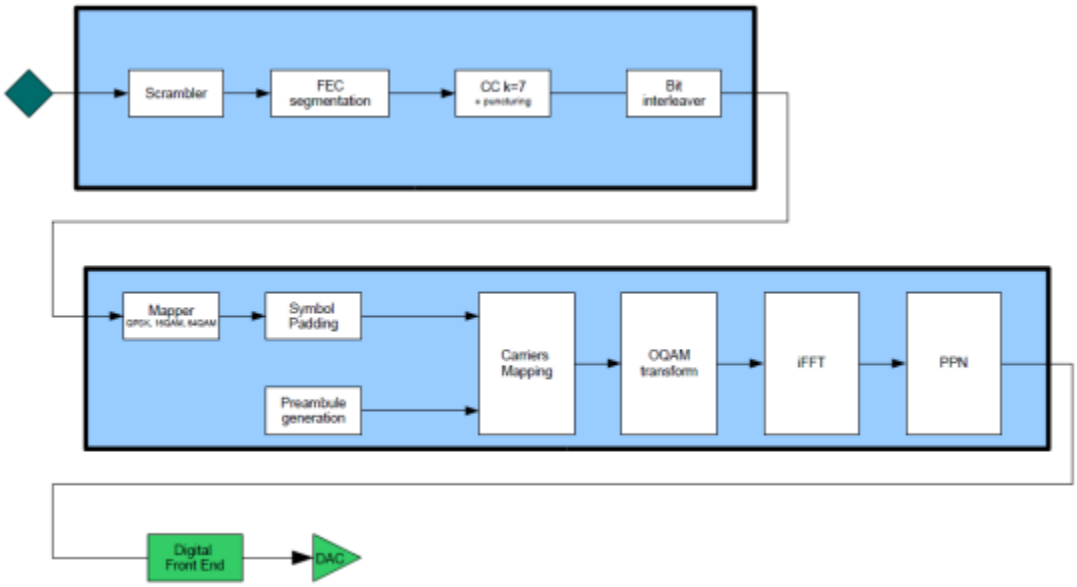


Figure 4-9. Architecture of the 5GNOW FBMC transmitter

The following section describes the baseband architecture of the FBMC transmitter along with the implemented algorithms.

The transmitter core architecture is composed of the following modules (see Figure 4-10):

- The Channel coding unit adapts the data to be sent to the constraints of the inner transmitter
- The inner transmitter implements the FBMC waveform generation
- The digital front end (DFE) transmitter adapts the sample rate of the signal at the output of the transmitter to the sampling rate and carrier frequency required at the DAC.

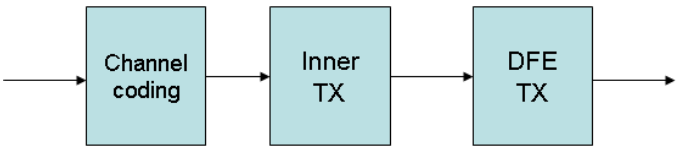


Figure 4-10. Structure of the TX core

The Channel coding processing block is composed of (see Figure 4-11):

- A 16 bits CRC,
- A scrambler to scramble the input data,
- A FEC block using a rate 1/2 mother code (convolutional code K=7) and different puncturing strategies,

- An interleaver to arrange subsequent encoded bit so that they are not sent in a non-contiguous way,
- Interleaved bits are then mapped to different constellations: QPSK, 16QAM, 64QAM after padding to fill all active subcarriers.

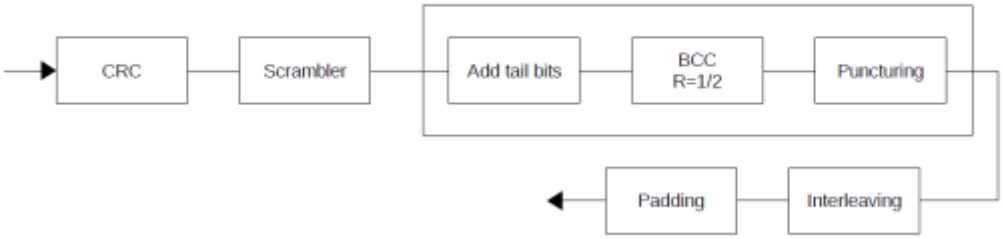


Figure 4-11. Channel coding structure

The inner transmitter is composed of two data branches. First the preamble data is inserted, and then data from the previous processing (Channel coding processing) is padded after mapping on active carriers. It should be mentioned that the mapping on active carrier is generic and can be configured on contiguous spectrum. After OQAM transform, data are then passed through the inverse FFT and the polyphase network (PPN) implementing the prototype filter of the FBMC waveform [Bel10]. The architecture of the filtering processing is depicted in Figure 4-12.

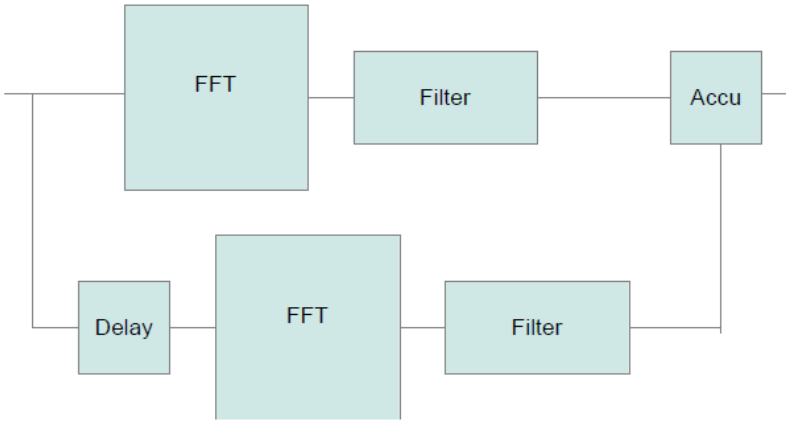


Figure 4-12. Architecture of the iFFT + filtering module

At the output of the inner transceiver, data is up-sampled from the output of inner TX to the sampling frequency expected at the input of the DAC. The operation is performed in 2 stages:

- First data is up-sampled by a factor of 7 (from 15.36 Ms/s to 107.52 MHz),
- Images are then filtered through a low pass filter,
- A fractional numerically controlled oscillator (NCO) converts by linear interpolation samples to the expected sampling rate at the input of the DAC (112 MHz).

Performance of the proposed DFE is depicted in Figure 4-13. We illustrate the frequency response of the DFE to an 8MHz band signal generated using a sampling frequency of 15.36MHz. The in-band ripple is lower than 0.5dB and images are rejected to more than 55dB.

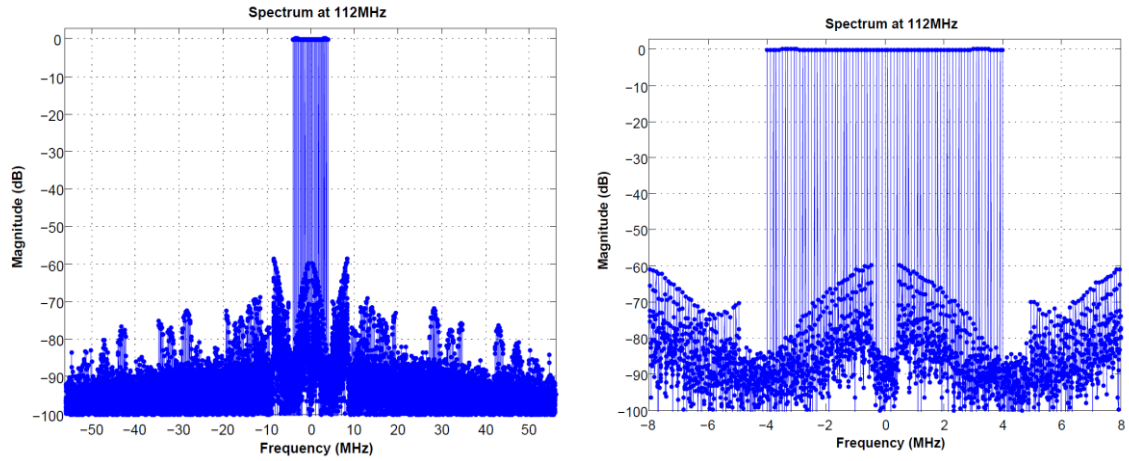


Figure 4-13. Illustration of the performance of the proposed digital front end

It should be mentioned that the IF (Intermediate Frequency) transposition is directly done by the DAC.

4.2.2 FBMC receiver

A flexible architecture for multiuser asynchronous reception on fragmented spectrum is able to exploit the advantages of FBMC if the signal is efficiently demodulated in the frequency domain without a priori knowledge of the FFT timing alignment (i.e. the location of the FFT block, this property is called asynchronous FFT). A receiver architecture based on this assumption is depicted in Figure 4-14. An asynchronous FFT of size KN is processed every blocks of N/2 samples generating KN points, i.e. if $\mathbf{r_m}$ is the m^{th} received vector, a KN-point FFT is computed for samples k = (n + m × N/2) with n = 0, 1, . . . ,NK − 1. These successive KN points are stored in a memory unit.

The detection of a start of burst is then achieved on the frequency domain (i.e. at the output of the FFT) using a priori information from the preamble. CFO is first estimated using the pilot subcarrier information of the preamble by computing the phase of the product between two consecutive FBMC symbols at the location of the pilot subcarriers. The propagation channel is assumed static for the duration of the burst. When large CFO correction is required, a first step in the estimation process consists of scanning the subcarriers around the pilot subcarrier locations to determine the subcarrier with the highest energy. A tracking algorithm of the CFO may complete the synchronization process when the duration of the burst is large and the accuracy of the preamble based detection algorithm does not meet the required level. CFO compensation is then performed in the frequency domain using a feed-forward approach.

The channel coefficients are then estimated on the pilot subcarriers before being interpolated on every active subcarrier. The use of a KN-point FFT makes the interpolation particularly specific to this receiver. The estimation of the channel coefficients is performed before applying the FBMC prototype filtering. The least square estimates of the channel coefficients are computed by applying a CFO phase correction on the received signal according to the location of the pilot symbol on the prototype filter. Performance may be further improved by considering all the positions of the prototype filter and by applying a maximum ratio combining algorithm after interpolation.
Once the channel is estimated on all the active subcarriers, a one-tap per subcarrier equalizer is applied before filtering by the FBMC prototype filter. Demapping and Log-Likelihood Ratio (LLR)

computation complete the inner receiver architecture. A soft-input Forward Error Correction (FEC) decoder recovers finally the original message.

The asynchronous frequency domain processing of the receiver combined with the high stop-band attenuation of the FBMC prototype filter provides a receiver architecture that allows for multiuser asynchronous reception. FFT and Memory Unit are common modules, while the remaining of the receiver should be duplicated as many times as the number of parallel asynchronous users the system may tolerate.

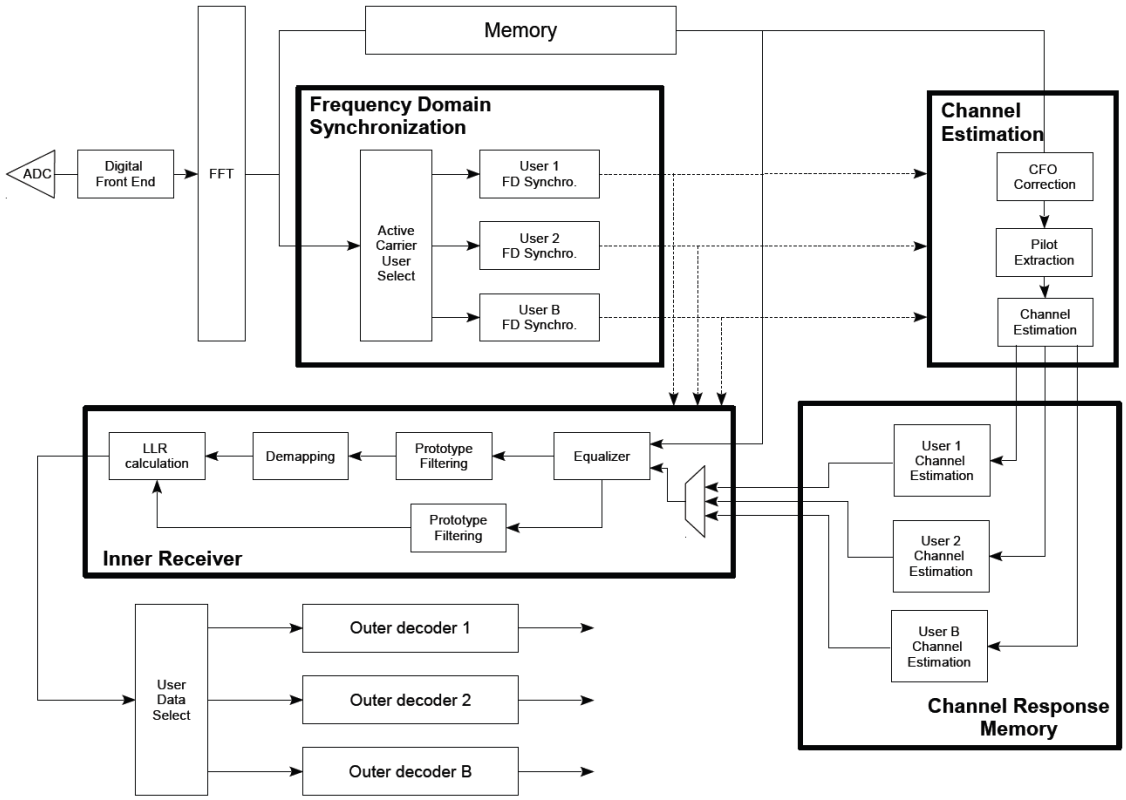


Figure 4-14: Block diagram of the proposed multiuser asynchronous receiver architecture

In the next sub-sections, details of the modules composing the baseband core receiver are given.

4.2.2.1 Digital Front End

The receiver digital front end is composed of:

- A rotor function implemented through a CORDIC algorithm that transforms the carrier modulated signal into I/Q baseband modulated signal followed by a low pass filter,
- A Fractional NCO/Resampler re-samples the generated signal to a multiple of the appropriate sampling frequency by linear interpolation (224Msample/s to 4x15.36Msamples/s),
- A decimation processing implemented through a symmetric real low pass filter (2x12 + 1 coefficients).

The input IF is set to 15MHz. Since the input rate is quite high (224Msample/s), we have limited to 7 the number of coefficient of the first low pass filter. The coefficients are equals to: [0.7698 0.6189 0.7433 0.7884 0.4733 0.6189 0.7698].

The performance of the proposed scheme is depicted in Figure 4-15. A fixed point model has been simulated and analysed. An 8-MHz band signal is generated with a sampling frequency of 224MHz. This signal is modulated around 15MHz (specified IF).

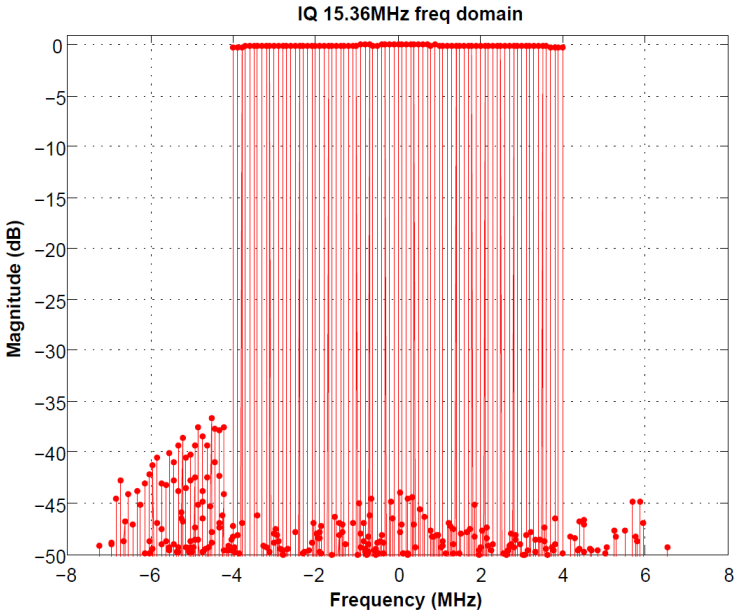


Figure 4-15. DFE RX performance

It should be noticed that the in-band (-4MHz to 4MHz) interference level is under -40dB. The out-band interference will be filtered in the frequency domain after FFT. The pass-band ripple is negligible.

4.2.2.2 FFT processing

After the DFE the signal is immediately send to the FFT. A 4096-point FFT is performed on the data flow every 512 samples. All the baseband processing is performed in the frequency domain. Since the number of active carriers is specified to be less than 512 the throughput at the output of the FFT is processing is around 61Msample/s (complex sample).

A pipelined streaming architecture based on Radix-2 butterfly processing engines has been implemented. A dynamic rescaling is performed at each stage to deal with “optimized” dynamic (see [Xil12] for more details). The architecture of the FFT is depicted in Figure 4-16.

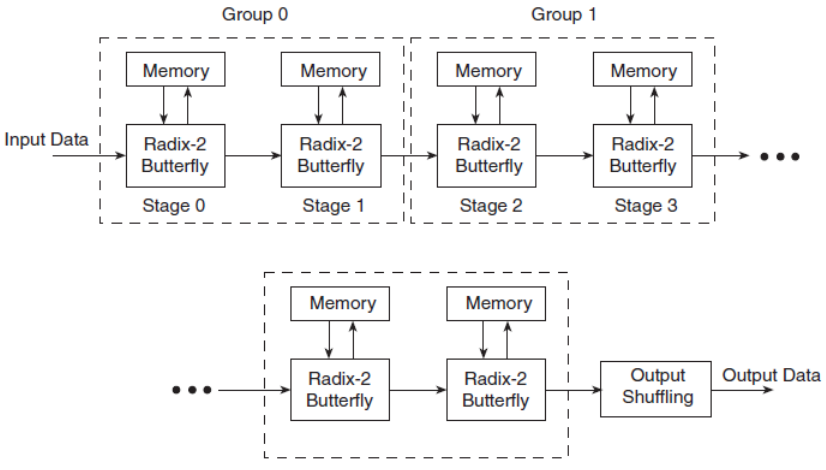


Figure 4-16. Illustration of the pipelined streaming architecture for the FFT (from [Xil12])

The output of the FFT is sent to a shared memory (for multi user extension).

4.2.2.3 Synchronization

The synchronization process is composed of two modules, the detection of the beginning of the burst and the Carrier Frequency offset estimation, as described below.

4.2.2.4 Burst detection

The detection of the beginning of the burst is performed on the frequency domain using pilot carriers.

4.2.2.5 CFO estimation

The estimation of the CFO is performed on the preamble. We compute the mean of the conjugate product between consecutive FBMC symbols on active carriers as depicted in Figure 4-17.

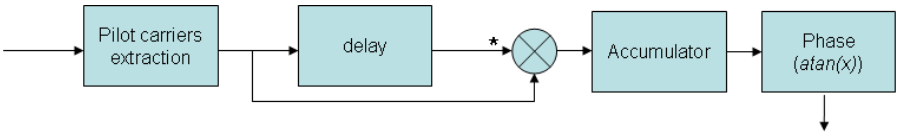


Figure 4-17. Architecture of CFO estimator

The phase of the complex number is calculated using the CORDIC algorithm. This algorithm was initially developed by Volder [Vol59] to iteratively solve trigonometric equations.

4.2.2.6 CFO correction

The correction of the frequency offset is performed on the frequency at the output of the shared memory. A low complexity ICI mitigation algorithm was proposed in WP3 and implemented in WP5. It means that the Inter Carrier Interference (ICI) generated by the CFO is mitigated along with a phase correction on FBMC symbols.

4.2.2.7 Channel Estimation

The channel estimation processor is composed of the following modules:

- An estimator. It estimates channel coefficient at the pilot location (depending on the preamble structure).
- An interpolator. Channel coefficients are then interpolated using a set of filter.

We have implemented the channel estimation algorithm studied in WP3.

In order to maximize the interpolation performance while maintaining a reasonable level of complexity, the interpolation architecture depicted in Figure 4-18 has been considered.

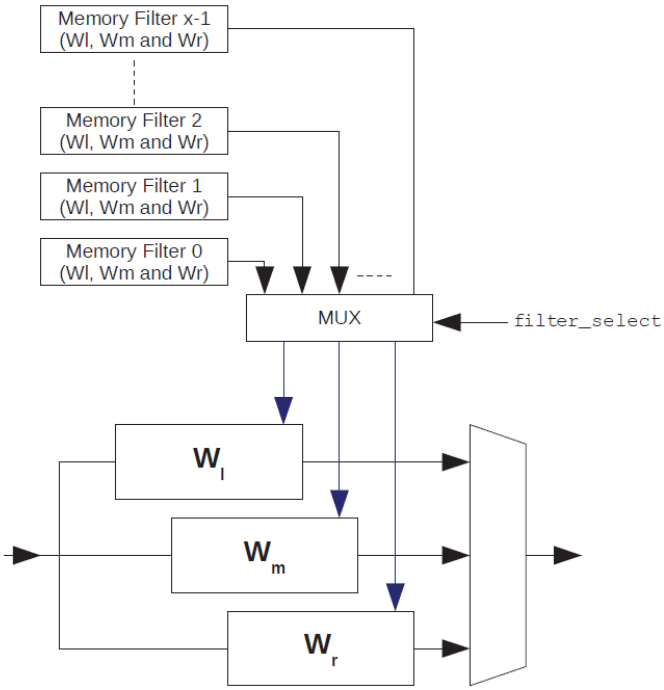


Figure 4-18. Architecture of Channel interpolator

A set of x filters is optimized according to a target Signal-to-Noise-Ratio (SNR), time domain channel duration, time domain profile, etc. W_l stands for the left edge filter, W_r for the right edge filter and W_m is middle filter. In practice x is fixed to 3. The choice of the filter to apply is controlled by an entity that estimates the received channel conditions and decides which filter suits most the channel conditions measured at the receiver. Estimated pilot carriers are fed through the three filter blocks and generate three interpolated channel estimates. The choice of the channel estimate is controlled by a multiplexer according to the subcarrier index.

4.2.2.8 Inner decoder

The architecture of the inner is decoder is “dataflow” oriented. First a classical ZF equalization is realized on each subcarrier. Samples at the output of the equalizer are then filtered by the prototype filter. The coefficients are: [0.2351 0.7071 0.9720 1 0.9720 0.7071 0.2351].

A decimation by a factor K=4 is then performed. Payload carriers are extracted and complex symbols are re-arranged to form QAM symbols (OQAM transformation).

A blind Signal to Noise ratio estimator has been developed to estimate the quality of the link. This estimator is based on the well know m2 m4 estimator. We have implemented biased estimator of the two moments (order 2 and 4) as illustrated in Figure 4-19. It should be noticed that the operation consisting in computing the SNR from the estimated moments is realized by the control software.

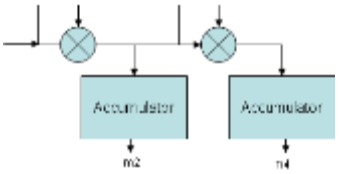


Figure 4-19 Architecture of m2 m4 estimator

We depict in Figure 4-20 the performance of the estimator for QPSK and 16 QAM constellations. The estimation is done on 4096 samples. It is clear that for 16-QAM modulation, the number of points for the moment estimation is too small; the variance of the estimated SNR is very high. It means that, for very short burst using high order modulation the estimator is not reliable.

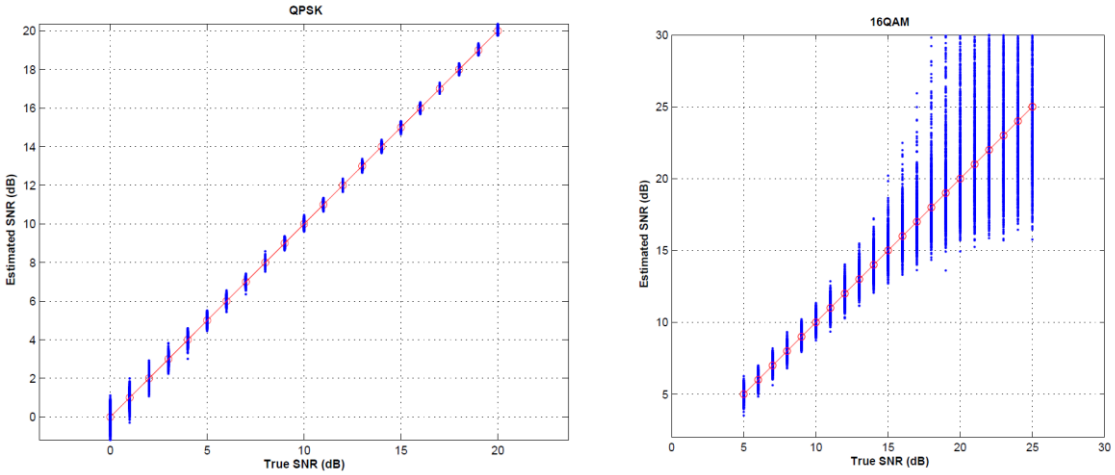
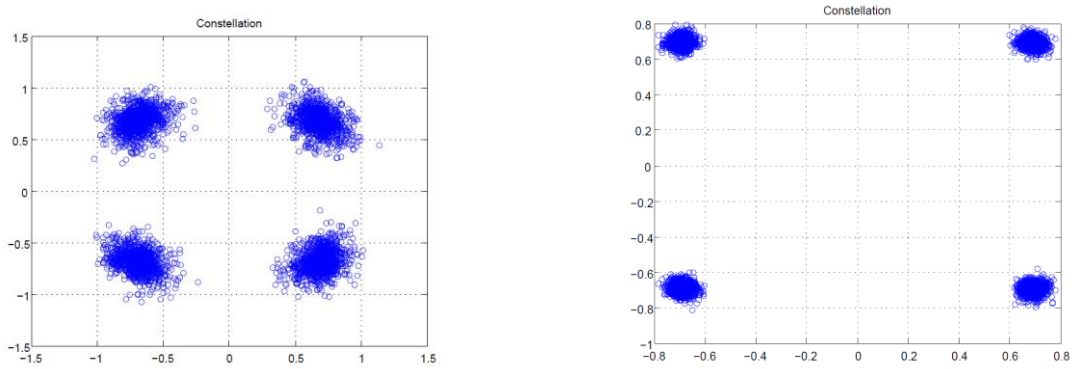


Figure 4-20. Accuracy of the proposed blind SNR estimator for QPSK/16QAM constellation

We have implemented a debug interface to monitor in real time the constellation of the decoded burst. Figure 4-21 illustrates the measured constellation for a FBMC signal. The estimated CFO is around 100Hz (0.67% of the sub-carrier spacing). Figure 4-21 (a) depicts the constellation when the CFO correction is bypassed, while Figure 4-21 (b) shows the constellation when the CFO correction is activated.



(a) (b)

Figure 4-21. Illustration of the measured constellation

De-mapping and Log Likelihood Ratio (LLR) computation is the last step of the inner decoding process. We have implemented a max-log approximation for symbol soft de-mapping (for more details please refer to [TB02]). The LLR are computed by scaling the output of the de-mapper by the channel coefficients.

4.2.2.9 Outer decoder

The outer decoder is composed of well-known interleaving and convolutional decoding modules. To be able to estimate the quality of the link we have implemented a blind estimator of the bit error rate at the input of the convolutional decoder (CBER: Coded Bit Error Rate). The architecture of the

convolutional code decoder is depicted in Figure 4-22. The output of the decoder is re-encoded and compared to the hard decision of the input data.

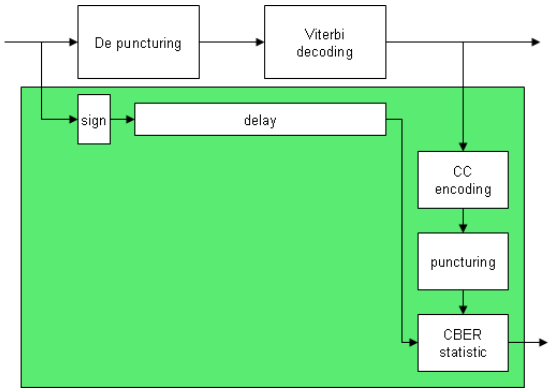


Figure 4-22. Architecture of the FEC decoding

A quite accurate estimation of the CBER is easily extracted. Figure 4-23 illustrates the performance of the proposed estimator for the three coding rates. When the CBER is lower than 10^{-2}, the proposed estimator is very accurate. Otherwise, we under estimated the CBER.

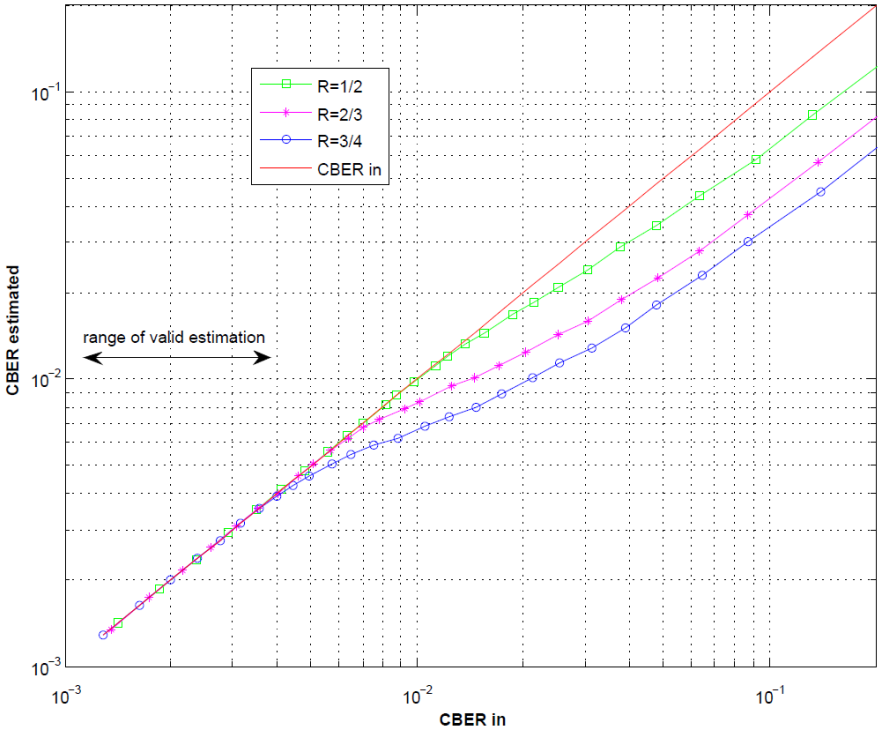


Figure 4-23. Illustration of the performance of the proposed blind CBER estimator

5 Evaluation of HW demonstrator concept

5.1 GFDM demonstrator platform

5.1.1 Complexity

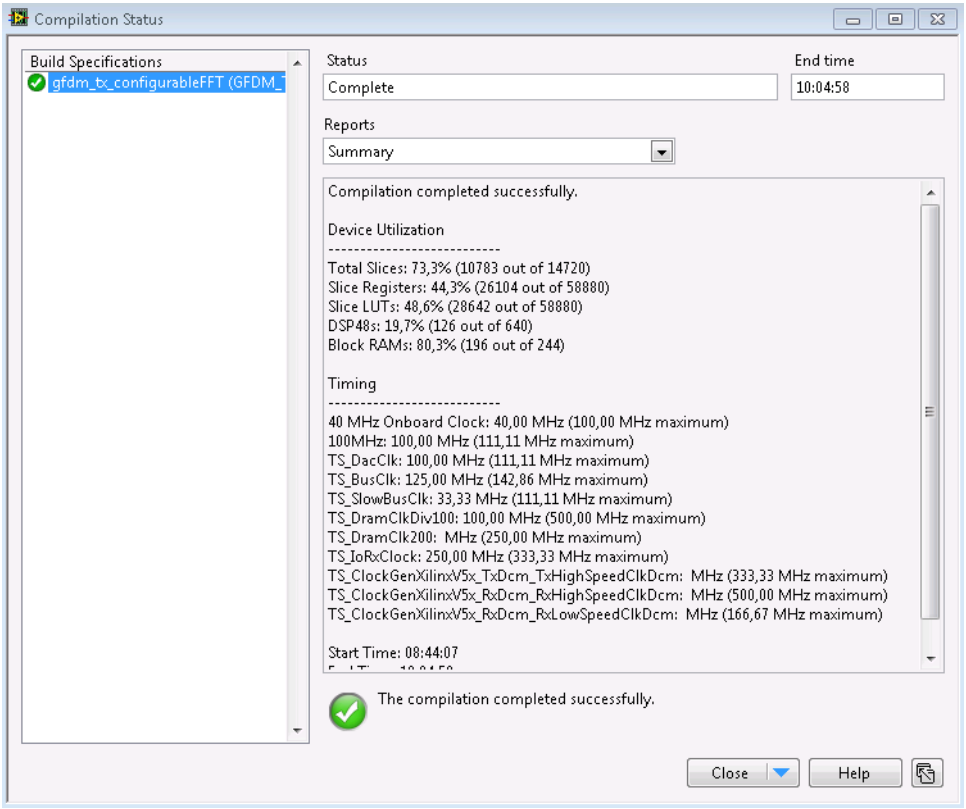
To verify the practical feasibility of the low-complexity GFDM transceiver structure, a software defined radio platform was designated for its implementation. The demonstrator consists of a National Instruments PXI PC-based platform including an Intel i7 general purpose processor (GPP) for controlling the application and performing basic baseband processing and a FlexRIO 7965 FPGA module for high-throughput baseband processing. NI FlexRIO provides user-programmable FPGA modules coupled to interchangeable I/O adapter modules, such as the NI-5791 RF transceiver module. The latter has continuous frequency coverage from 200 MHz to 4.4 GHz, 100 MHz of instantaneous bandwidth on both transmitter and receiver, and performs signal up- and down-conversion to and from radio frequencies. The hardware and software components of this platform are integrated with the LabVIEW graphical programming language.

The GFDM transceiver was fully implemented on the FPGA of the platform, realizing the pipeline structure as described in this section. The parameter configuration in the GUI, Figure 5-2, is flexible, which allows covering a variety of different GFDM applications.

The GFDM implementation makes use of the Xilinx FFT IP core. This IP core supports a pipelined streaming architecture for continuous data processing and a run-time configurable transform point size that can be a positive integer power of two. Compiling the GFDM transmitter for a Xilinx Virtex-5 SX95T FPGA platform uses around 75% of the chip resources. The digital baseband processing uses a parallel structure with different timed loops and a first-in-first-out (FIFO) memory approach to exchange data among processing blocks.

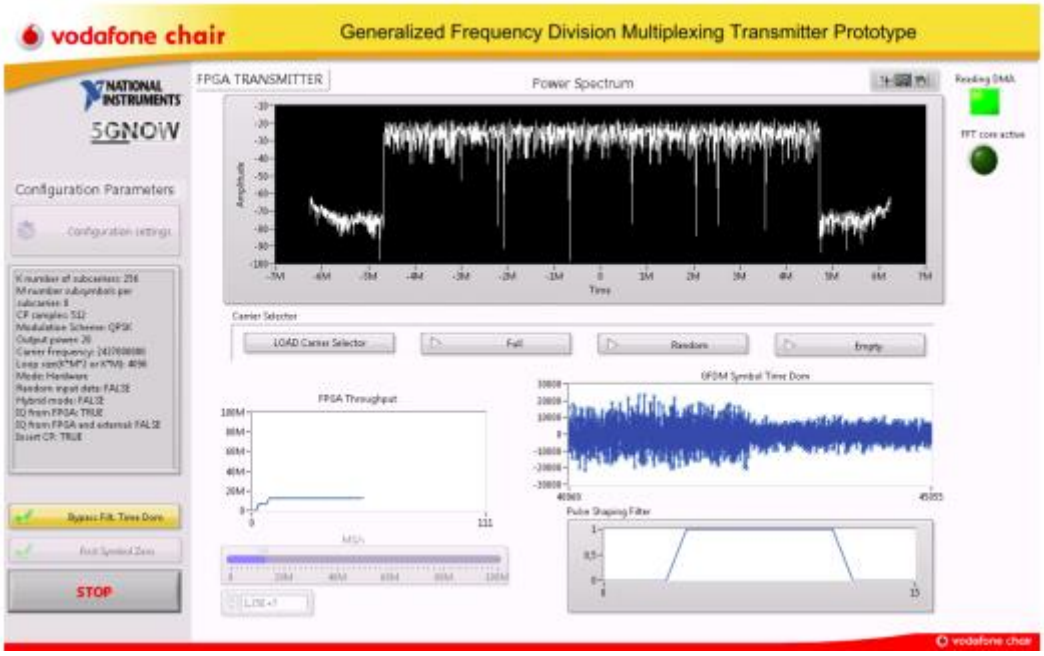
It is worth noticing that the design also includes advanced debugging features that allow collection of internal data and the control of system parameters through an external graphical user interface (GUI) developed with LabVIEW. The bottleneck in the system is the loop that feeds the DAC. With typical bandwidths being in the range between 20 MHz and 50 MHz, the current design is capable to generate GFDM blocks of up to 32768 samples length continuously.

The complete base implementation verifies that GFDM can be implemented with reasonable complexity using today's technology. The prototype is the core of a more general 5G wireless testbed for experimental research and will be extended by more advanced algorithms and additional PHY layer features, such as framing, channel coding, and data interfaces in the future.

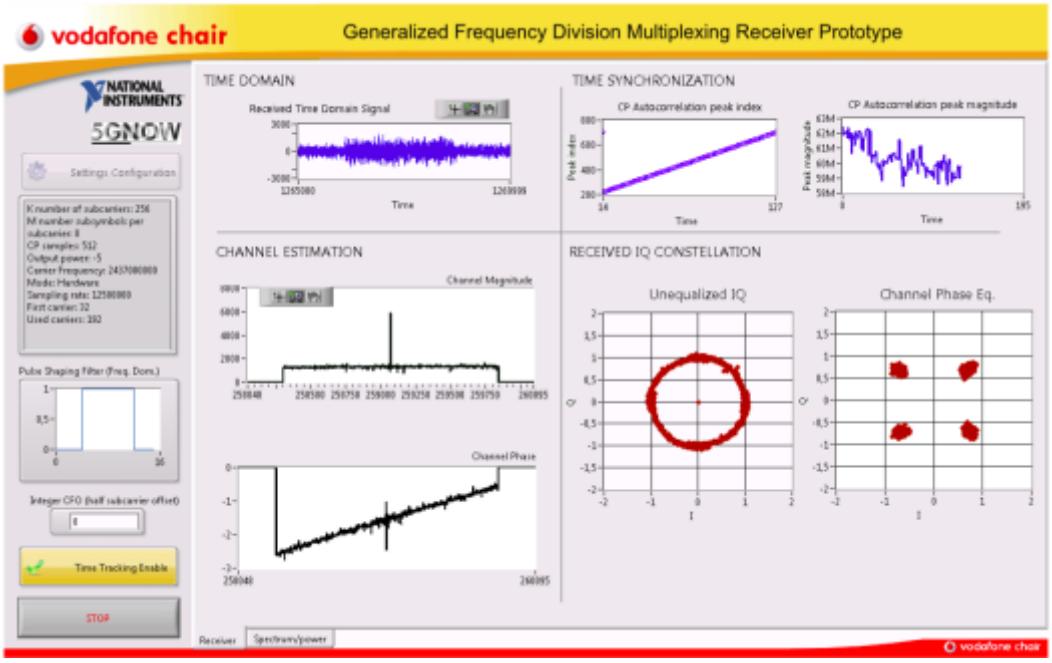


Resources	Value
Total Slices	73,3% (10783 out of 14720)
Slice Registers	44,3% (26104 out of 58880)
Slice LUT	48,6% (28642 out of 58880)
DSP48s	19,7% (126 out of 640)
Block RAMs	80,3% (196 out of 244)

Figure 5-1 GFDM Transmitter compilation results



(a)



(b)

Figure 5-2 GFDM Transceiver GUI, (a) transmitter, (b) receiver

The LabVIEW code has been made available at:
https://mns.ifn.et.tu-dresden.de/Research/Projects/Pages/5GNOW.aspx

5.1.2 Hardware in the Loop approach

The low complexity FPGA implementation cannot at the current phase reproduce all the flexible and advanced algorithms envisioned for GFDM. An alternative implementation based on higher level scripts, e.g. Python, Matlab, LabView, etc. has been developed as a solution for addressing more advanced features in a non-real-time principle.

The concept termed as hardware in the loop (HALO) uses the available equipment to transmit pre-compiled test vectors in a repetitive manner. On the receiver side the over the air transmitted signal will be distorted by the channel, noise and interfering signals.

The setup is assisted by a communication library that allows the transmission of the test vectors using an user datagram protocol (UDP). A single DLL file has been tested with Python, Matlab, Labview. Configuration can be achieved through GUI or via TCP write command works, with up to 30M double values (~240 MB) per block. The library contains the same commands for NI USRP, PXI-System (with possible extension for other devices). This setup is illustrated in Figure 5-3.

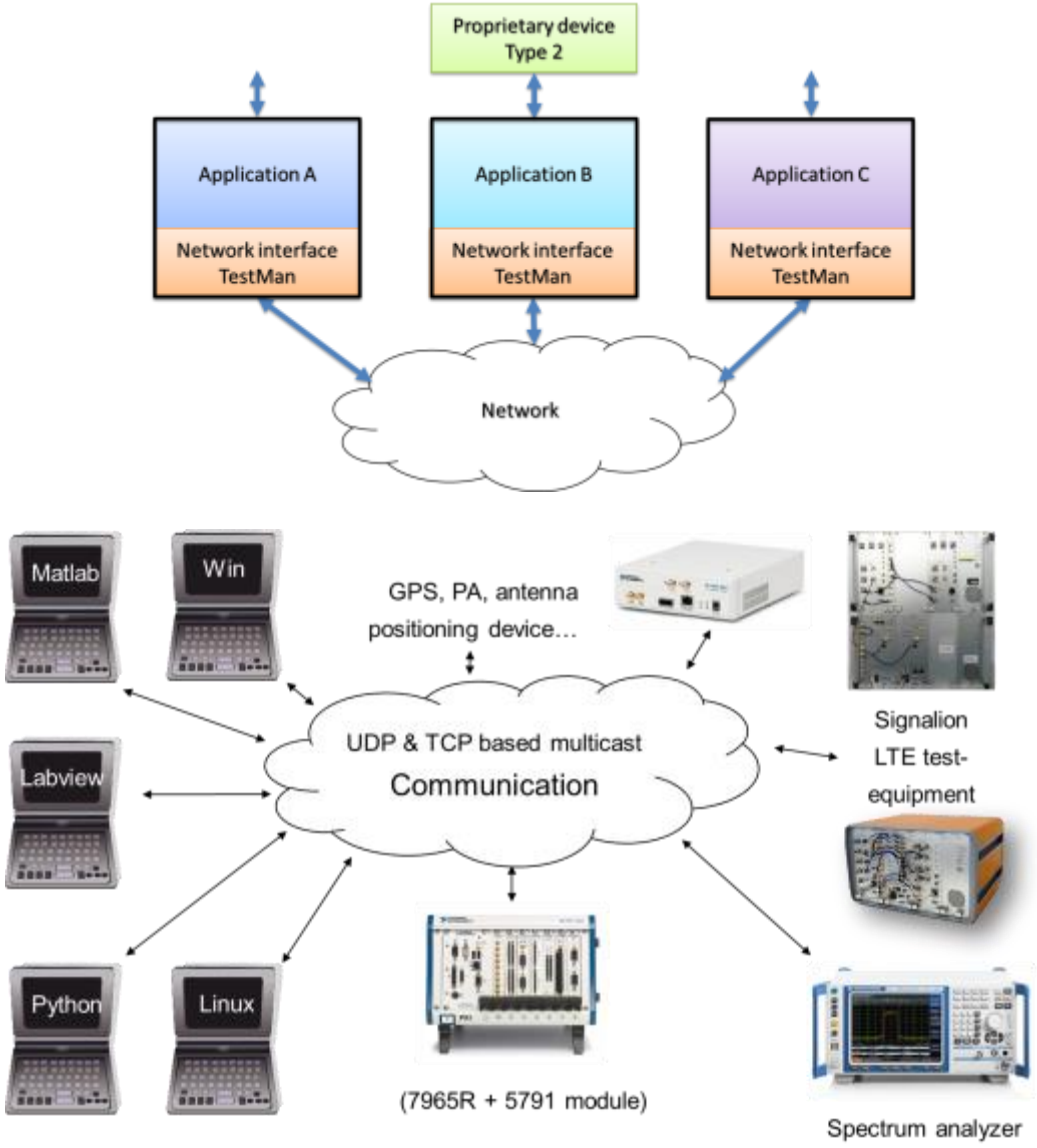


Figure 5-3 HALO setup

The advantage of UDP multicast is that messages can be sent in a decentralized way to all computers in a network. So it is not needed to setup a common server to distribute information's between all peers. Once an Application is started it is ready to work. Another advantage is that the UDP multicast packets can be received even in different IP ranges. It is also the main disadvantage because a network can easily be flooded and overloaded. As a result TCP peer to peer connections are introduced for sharing higher amounts of data. (The UDP communication is used to share IP addresses and ports between the applications.)

To distinguish between different applications a type and an ID are introduced for each application. So it is possible to group similar applications together and the DLL can filter out messages which are intended for other applications.

5.2 FBMC demonstrator platform

The evaluation of the FBMC demonstrator platform is done according to some of the reference scenarios given in section 2.1, namely single user link and multiuser uplink.

The complexity of the TX core is illustrated in Table 5-1. As expected, the complexity of the TX core is dominated by the iFFT and filtering processing.

	Slice Register	LUTs	DSP48E1
Scrambler	29	22	0
FEC segmentation	95	110	0
FEC	61	26	0
Interleaver	134	167	1
Padding	81	77	0
Mapping	70	62	0
Carriers mapping	1108	603	0
Preamble insertion	3553	1880	0
FBMC processing (including iFFT)	10662	7734	106

Table 5-1. Complexity of the differents parts of the TX core

We depict in Figure 5-4 the complexity of the FBMC processing module. The complexity is dominated by the two iFFT modules. It should be mentioned that it is possible to optimize the architecture by considering only one iFFT processor working at a higher frequency clock. Despite the complexity reduction, this kind of architecture imposes higher constraints on the clock frequency and more complex control.

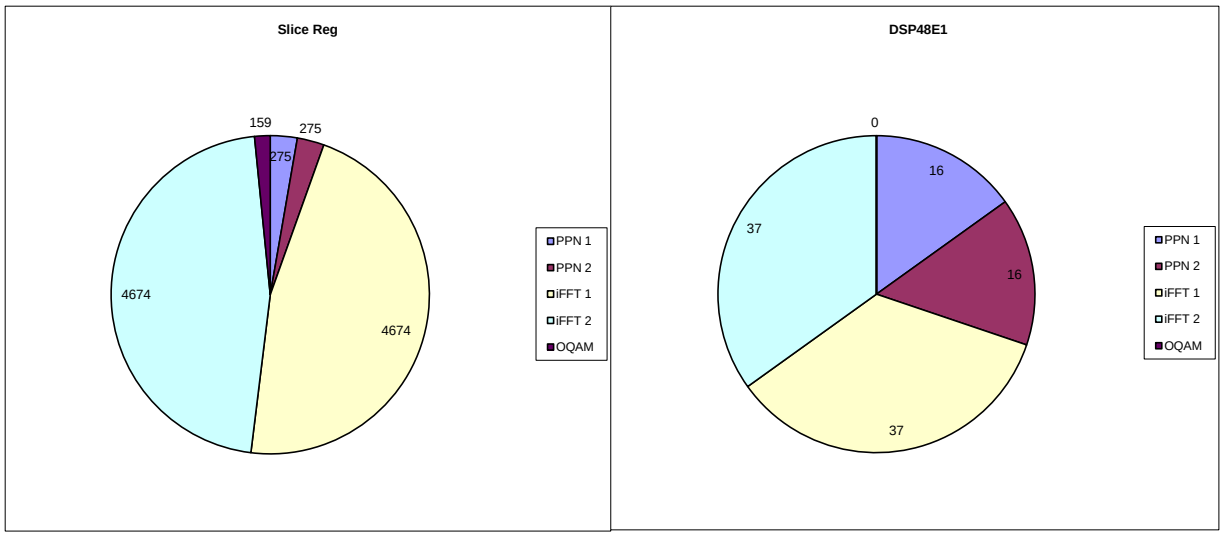


Figure 5-4. Complexity of the FBMC processing, iFFT + PPN filtering

By considering these complexity measures, it is possible to compare the complexity of OFDM and TX FBMC TX. We assume that for an OFDM transmitter only one iFFT is required (the complexity of the guard interval insertion module is negligible). By using complexity metrics of Table 5-1 and Figure 5-4, the complexity of a FBMC TX is increased by a factor 1.5 compared to OFDM complexity (Estimated Slice Register complexity of OFDM is assumed to be 4674):

Complexity factor = (sum(Slice Reg[Table 5-1])- 10662 + 4674) / sum(Slice Reg[Table 5-1])

= 1.4812

However FBMC waveform allows better frequency localization and enables asynchronous processing. All these parameters should be balanced.

The multiuser receiver architecture has been implemented on a Xilinx Kintex-7 (XC7K325T) FPGA of a T-FleX platform [Dor14] for a total of 2 users. Because of the limited amount of functions dedicated per user, the results can be scaled for more users. Resource usage of the mapped receiver is studied in terms of Slice Registers (Slice Regs), Look-up Tables (LUTs), DSP Blocks (DSP48E1) and memory banks (RAM Blocks) used by the different functions of the design. Slice Registers correspond to the number of register cells used, while Look-up tables to the amount of combinatorial logic in the design. DSP48E1 cells are combinatorial logic cells dedicated to multiplication and accumulation (DSP) operations. Memory banks correspond to the overall amount of storage required by the design. The designed has been mapped using a 130MHz clock frequency for the FPGA. The receiver is designed for the 10MHz LTE parameters, i.e.: FBMC carriers are separated by 15kHz, the overall bandwidth of the receiver is equal to 10MHz. The implementation is designed to receive any aggregation of resource block (i.e. 12 consecutive carriers) inside a 10MHz bandwidth sent by the two non-synchronized user equipment terminals. Out-of-band signaling sets the configuration of each user equipment (i.e.: which frequency resource blocks are allocated for each user). The complexity of the mapped design is summarized in Table 5-2.

Function	Resource Utilization			
	Slice Regs	LUTs	DSP48E1	RAM Blks
Digital Front End	11340	9041	46	0
FFT	6610	4481	19	35
Memory	594	628	2	100
FD Synchro.	10527	14437	60	6
Channel Est.	16125	12352	53	12
Channel Resp. Mem.	182	96	0	4
Inner Receiver	13195	11946	46	7
Outer Decoder	4878	10968	2	16
Control	35193	17210	0	3
Total	98644	81159	228	183

Table 5-2. FPGA hardware resource utilization for a 2-user receiver.

The design meets the hardware constraints of the Kintex-7 available on the T-FleX platform (XC7K325T). However, more than the actual absolute figures, the relative complexity is also interesting to analyze. Table 5-3 gives the relative complexity of the main functions of the 2-user receiver. Control and Channel Estimation take around a half of the necessary slice registers. The flexibility of the design and notably the ability to detect any resource block within the 10MHz bandwidth of the receiver explains this overhead of complexity. Furthermore, channel estimation has been implemented using interpolation technique based on interpolation filters. The coefficients of the filter have been left programmable for better flexibility. The memory block accounts for more than half of the memory in the receiver design (55%) while the FFT is the second largest function in terms of memory requirement (15% of the memory). The blocks that are duplicated to be able to address more than one user at the same time (FD synchronization, channel response memory and outer decoder) only account for 16% of the slice registers, 31% of the LUTs and 14% of the memory blocks.

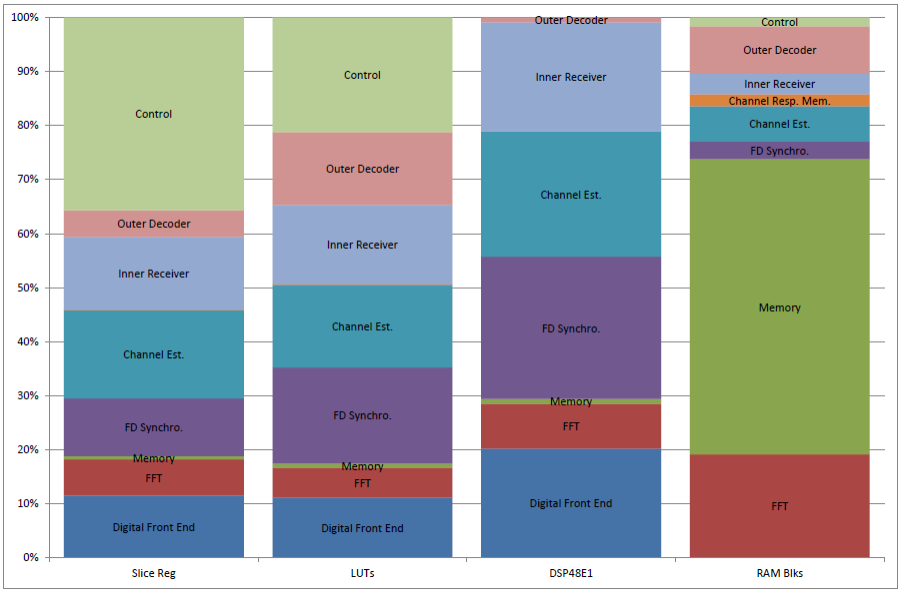


Table 5-3. Relative FPGA hardware resource utilization for a 2-user FBMC receiver.

These results show that the complexity of an FBMC asynchronous receiver can scale to address multiple users at the same time. The level of complexity is more dependent on the bandwidth addressed by the receiver than the number of asynchronous users being detected at the same time. This comment is valid for a small number of users, but as the number of users is increased, useful data rate per user is decreased and duplicated operation could benefit from hardware resource

sharing. Practical implementations of FBMC in multiuser asynchronous frequency division multiple access mode is therefore possible on Kintex-7 FPGA platforms.

Table 5-4 compares resource utilization of FS-FBMC with OFDM receivers, in the single user case. Digital logic occupancy is similar while memory usage is significantly increased. In terms of digital logic, FBMC takes around 30% extra area in comparison to OFDM. However, memory usage is almost multiplied by a factor of 4. This is directly proportional to the overlapping ratio (*K*) of the FBMC prototype filter. In actual implementations, the computational overhead is only in the order of 30%. However, with FS-FBMC memory usage is significantly increased (3.5 times). This is due to the fact that computational complexity was limited thanks to a resource sharing strategy, which comes at the cost of storage. However, it is worth mentioning that memory cost in submicron technology is limited and can be easily traded against the benefits of FBMC in terms of dynamic spectrum access flexibility.

Function	Resource utilization Xilinx Kintex-7 (XC7K325T)			
	Slice Regs	*LUTs*	*DSP48E1*	*RAM BLKs*
OFDM				
FFT	5131	3815	13	10
Inner Receiver	24440	19540	75	22
Fec Decoder	2439	5493	1	8
Control	10564	10762	8	9
OFDM Total	42574	39600	97	49
FS-FBMC				
FFT	6615	4394	19	35
Inner Receiver	32710	26756	125	90
Fec Decoder	2439	5493	1	8
Control	13206	13453	10	38
FS-FBMC Total	54970	50096	155	171
FS-FBMC / OFDM resource usage ratio	1.29	1.27	1.60	3.49

Table 5-4. Hardware resource utilization – Comparison: OFDM vs FS-FBMC receiver

The table below reminds the main properties of FBMC.

BER	Similar to CP-OFDM
PAPR	Similar to OFDM (LTE-A)
Out of band radiation	Very well localized spectrum, up to -55dB attenuation at adjacent subcarriers
Throughput	Higher throughput due to cyclic prefix removal
Spectral efficiency	Supports OQAM modulations, high spectral efficiency due to cyclic prefix absence and lower side lobes
Complexity	FFT/IFFT structure, higher complexity than OFDM (polyphase network)
Training structure	Burst modes with preambles allows time-frequency synchronization and channel estimation

Sensitive to time and frequency offsets	Very robust to time and frequency offsets
Multiuser capability	Adapted to asynchronous users scenario
Multipoint capability	Avoid multiple access interference in uplink, less complex than equivalent CP-OFDM with MAI-cancellation, better than OFDM for given scenario with impairments (e.g. precision of local oscillators)
Resource allocation mechanisms/ channel adaptive scheduling	LTE like
Adaptivity potential	Flexible parameters: number of symbols per subcarrier, number of subcarriers, …
Coexistence to legacy systems	Low out of band radiation
Key open problems	Frame/frameless structure, synchronization, channel estimation (fragmented spectrum) and equalization
Test environments	Single/parallel-user links with AWGN and multipath channels
Implementation/demonstrator of waveforms	CEA-LETI platform (FPGA/ARM-cortex8) and NI RF front-ends
Intrinsic motivation for	Explore the advantages of well-localized spectrum and increase of spectral efficiency. Keep the advantages of LTE in not so synchronous and orthogonal scenario

Table 5-5. Main properties of FBMC

During FuNEMS 2013 (3-5 July, Lisbon), CEA presented its reconfigurable FPGA/ARM digital baseband platform implementing fragmented spectrum processing both at transmit and receive parts using FBMC modulation (see Figure 5-5). This real time HW platform aims at demonstrating the FBMC built-in filtering feature adapted to spectrum availability in the fragmented case. An important result is that the complexity of FBMC implementation is contained and may be demonstrated on a single FPGA (small form factor of 160 * 78 * 43 mm).

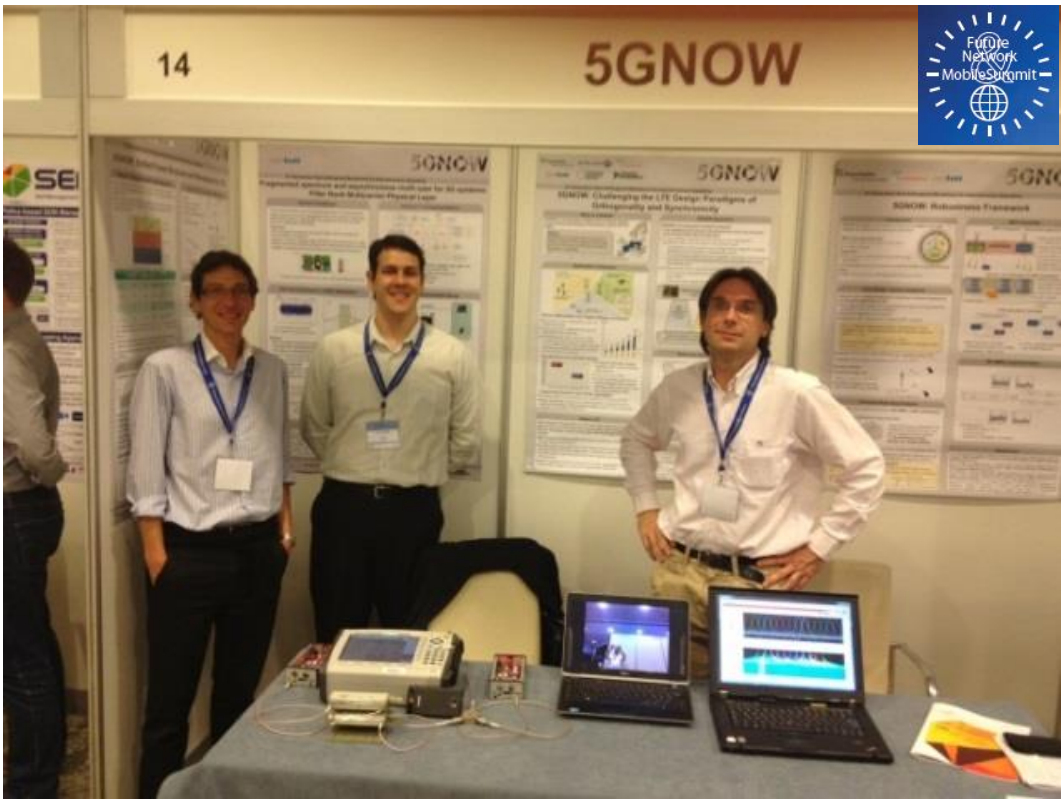


Figure 5-5. Picture of 5GNOW booth at Funems 2013

The first step was to demonstrate a point to point transmission with fragmented spectrum access. The synoptic of the demonstrator used during FuNEMS event is given in Figure 5-6, while the fragmented spectrum under consideration is given in Figure 5-7.

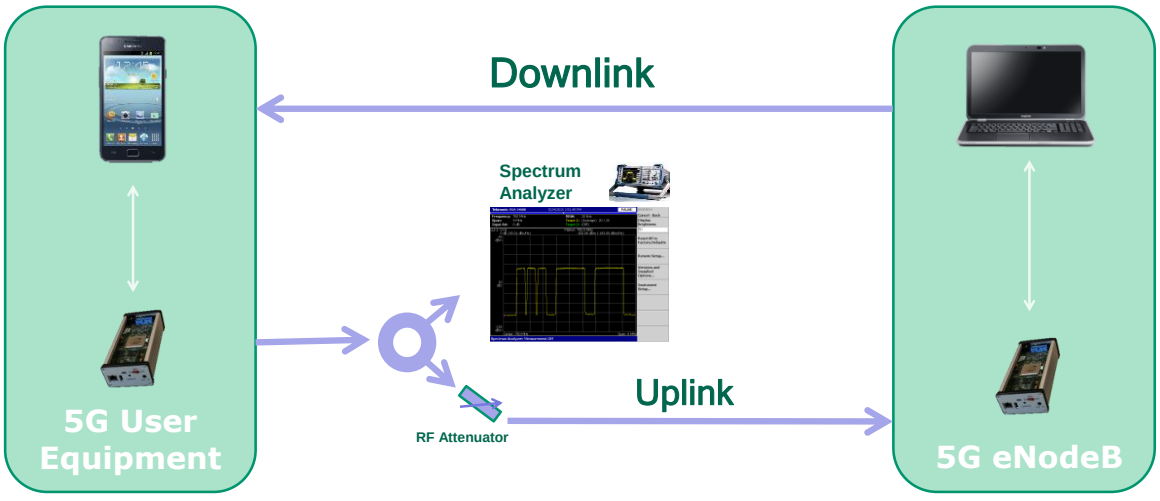


Figure 5-6. Synoptic of the FBMC demonstration at FuNEMS 2013

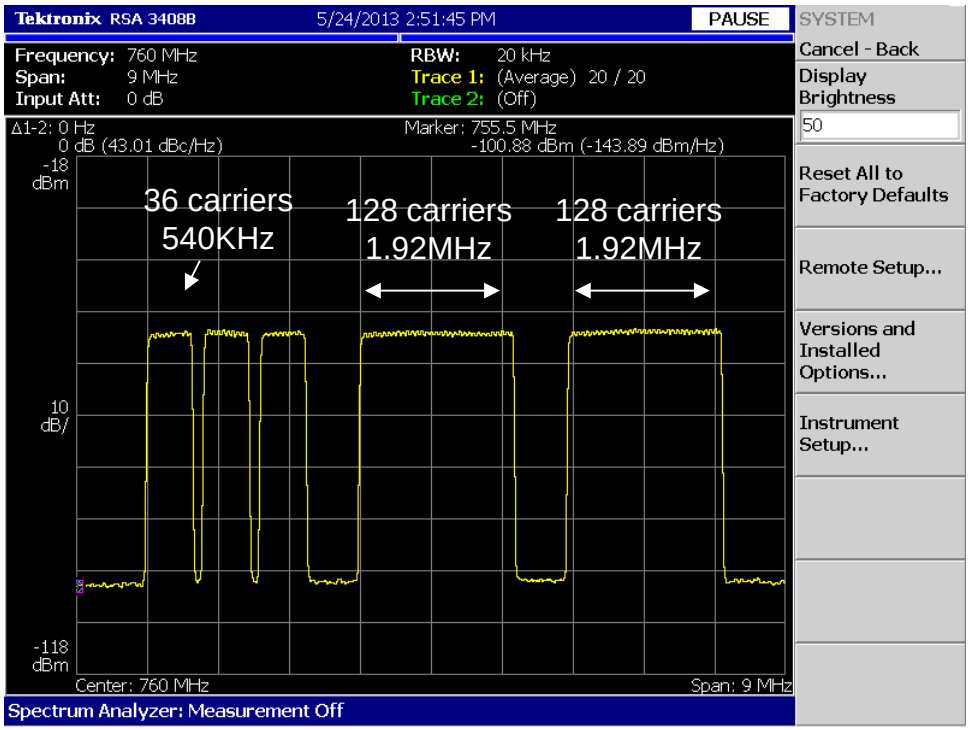


Figure 5-7. Fragmented spectrum used for the demonstration

During EuCNC'14 (Bologna, 23-26th June 2014), CEA-Leti assessed the performance of a multi-user transmission performance in presence of adjacent asynchronous transmitter in a fragmented spectrum context. Simulated results were validated through real experimentation:

- Fragmented spectrum usage is addressed in baseband: FBMC built-in digital filter of filterbank modulation allows for spectrum pooling of resource blocks
- FBMC consistently outperforms OFDM when two users are not synchronized
- FBMC-MA can be considered for dynamic spectrum access in a fragmented spectrum context

The eNodeB receiver was evaluated in presence of asynchronous adjacent user (OFDM or FBMC). Asynchronous fragmented spectrum access is considered for both terminals UE1 and UE2. Baseband UL transmitter/receiver are implemented on FPGA platform. Radio frequency up- and down conversion are performed using NI PXI modules. UE1 and UE2 transmit signal in different frequency bands. Users are not synchronized in time, a frequency offset between the two UEs is considered. The conclusion is: as expected OFDM generates more interference than FBMC. Quality of Service can be guaranteed with FBMC, but not with OFDM.

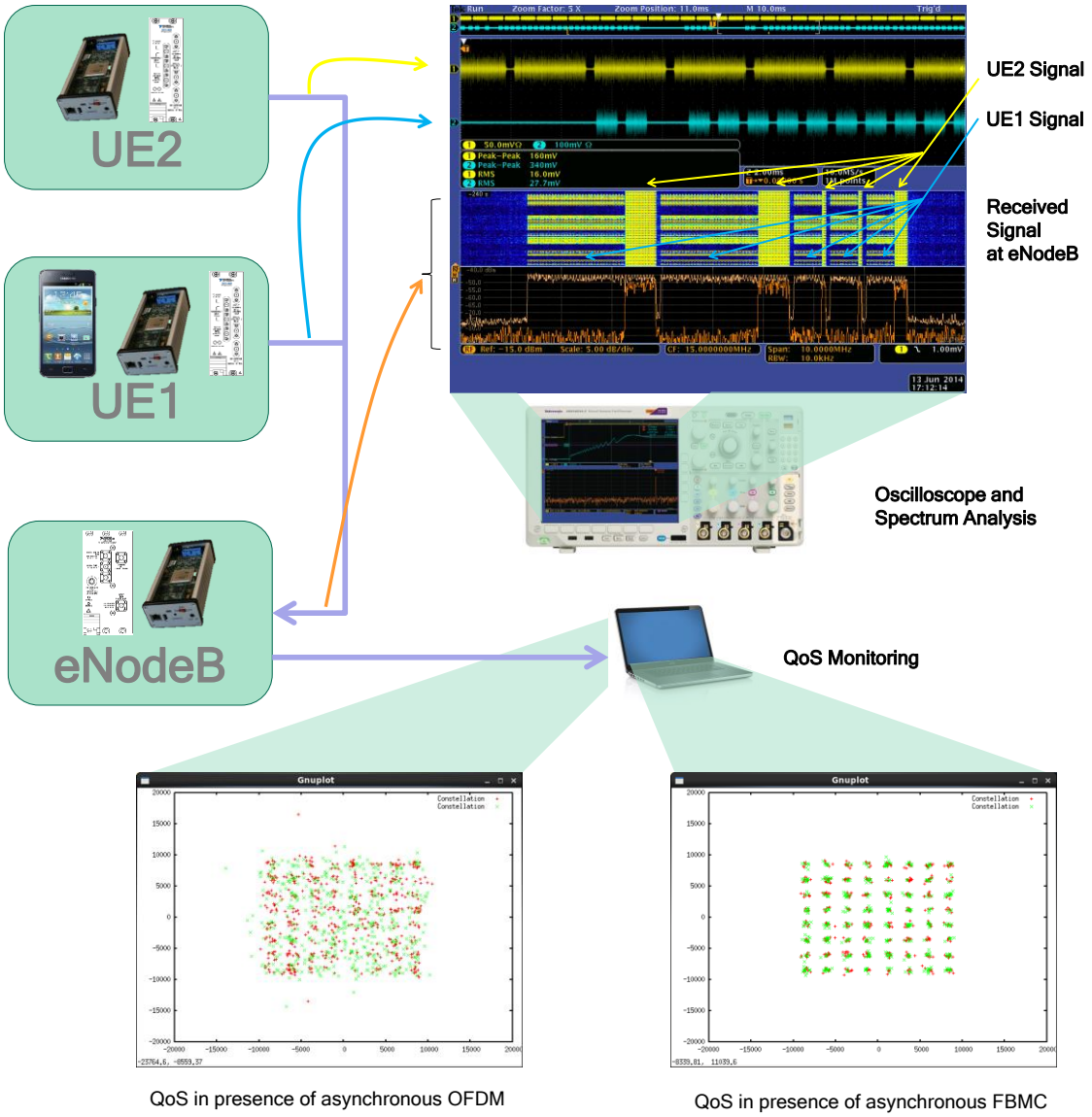


Figure 5-8. Overview of the demonstation and performance results

5.3 Joint demonstration with HALO approach

Using the HALO approach a 'test vector' based evaluation of GFDM and FBMC is going to be prepared according to Figure 5-9.

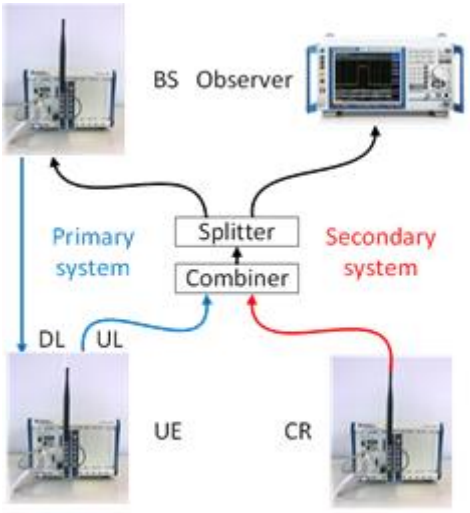


Figure 5-9 Joint demo setup

The concept to be explored is that FBMC will be defined as a secondary system in one part and GFDM in as a primary one in the other part, positioning the active carriers as UL fragmented spectrum access (LTE – 10MHz BW).

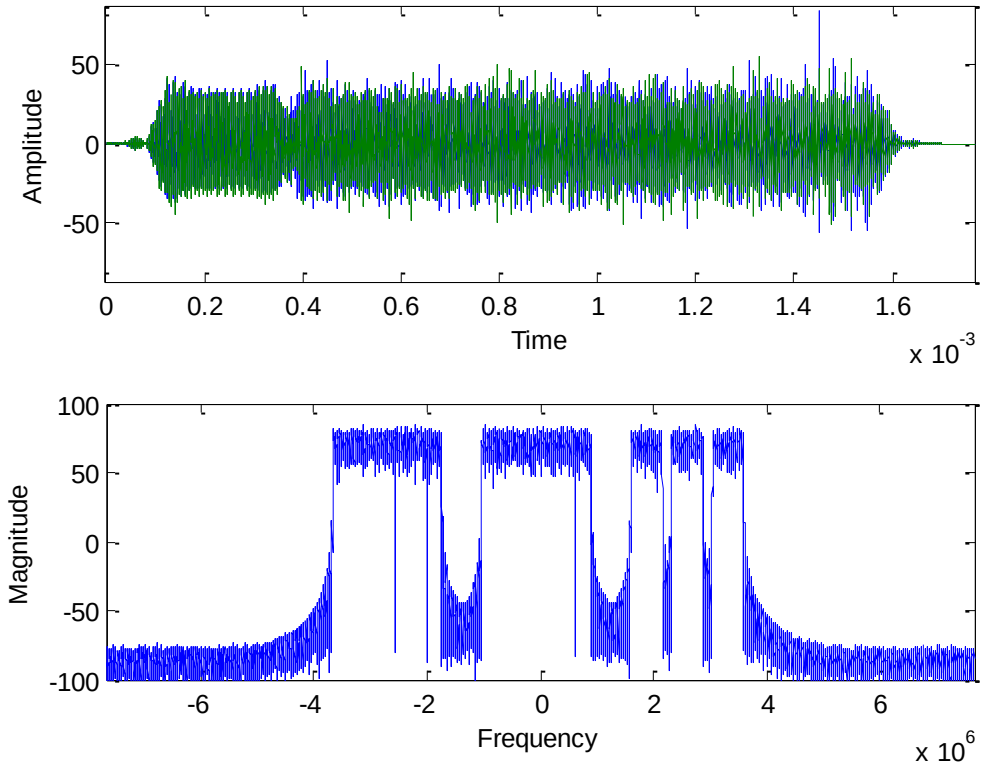


Figure 5-10 FBMC test vector: Sampling freq.: 15.36MHz, Burst length: ~1.6ms, Subcarrier spacing: 15kHz

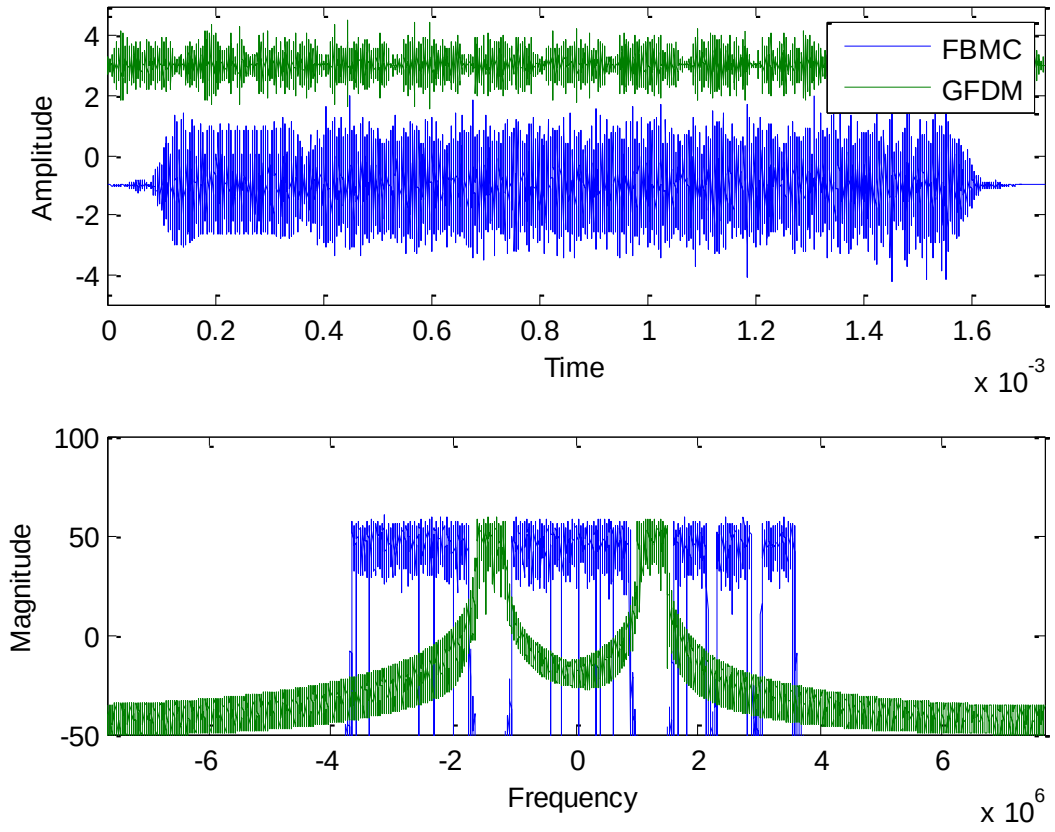


Figure 5-11 GFDM and FBMC test vectors

GFDM proposed configuration will follow the parameters introduced in Figure 2-4 (b) for a configuration aligned with the LTE grid:

Pulse shape: 'raised cosine'

Roll-off: 0

Number of CP samples: 128

Modulation: QPSK

Number of transmitted blocks: 13

Number of subcarriers: 128

Number of subsymbols per subcarrier: 15

Active subcarriers set: [51 52 53 54 73 74 75 76]

All devices will be connected via cables to control the transmission environment. The GFDM transmitter will be combined with an interfering FBMC transmitter. This combined signal will be divided for a spectrum analyser monitoring system and for the GFDM receiver by a power splitter. Every transmitter port has enough attenuation to prevent clipping at the receiving side. The power difference between the primary and secondary will be changed and the receiver characteristics evaluated in terms of Modulation error vs out of band leakage.

5.4 Real-time demonstration of the coexistence between a LTE legacy link and an asynchronous GFDM user

As stated in section 2.1 one of the reference scenarios addressed by 5GNOW is the scenario of parallel asynchronous single user links. Of special interest is the coexistence between a LTE legacy link and an asynchronous parallel 5G user. To demonstrate and explore the capabilities and benefits of the use of non-orthogonal waveforms in such scenarios a complementary real-time demonstrator has been developed. It is based on National Instrument's real-time capable prototyping platform. A sketch of the transmission setup is shown in Figure 5-12.

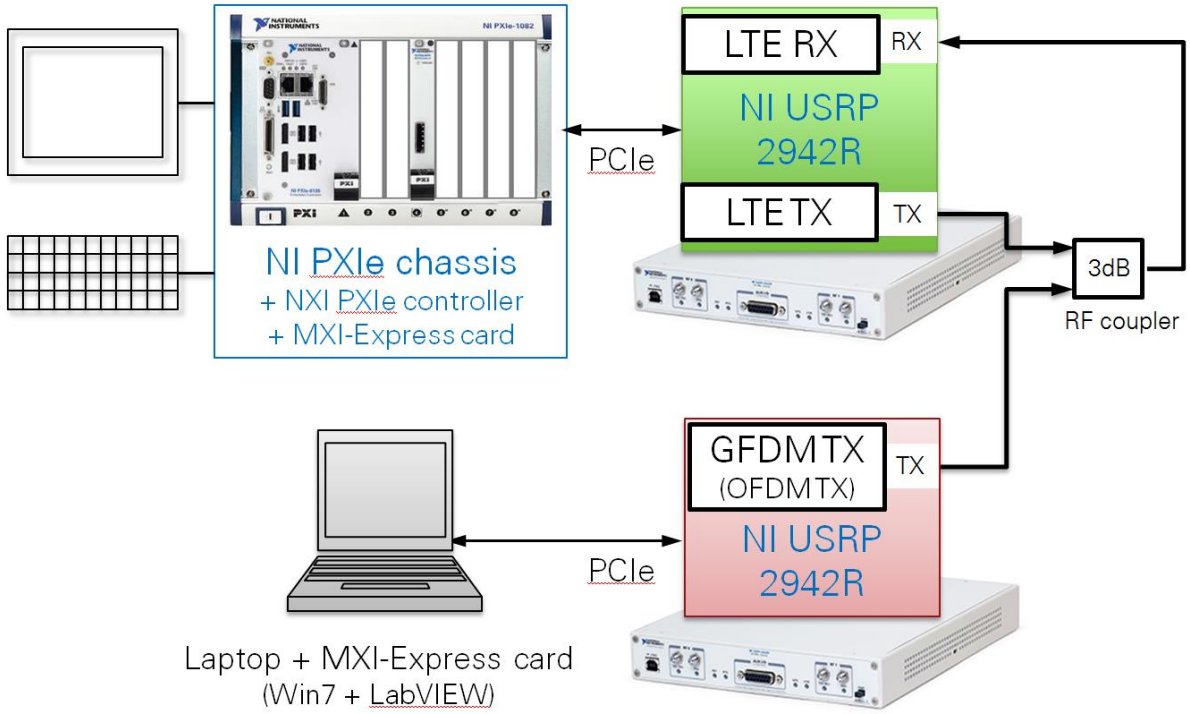


Figure 5-12 Real-time demonstrator setup for exploring the influence of an asynchronous GFDM user onto a LTE legacy link

This demonstrator setup makes use of National Instruments USRP-2942R devices (for details see section 3.1.5). As described in section 3.1.5 the USRP-2942R provides a software-defined radio platform which combines a dual RF transceiver (RF frequency range: 400MHz-4.4GHz) with a user programmable Kintex-7-FPGA. In the demonstrator setup the USRP-2942R devices are connected via a PCI Express connection with either a laptop, or a NI PXI chassis hosting a NI PXI embedded controller. Figure 5-12 exemplarily shows both options.

The legacy LTE link of the demonstrator is realized by a LabVIEW based LTE application software which has been developed by National instruments. This LTE application software provides a LTE downlink compliant physical layer (including both transmit and receive side) with the following system features and parameters:

- General modulation scheme: OFDM (compliant to LTE downlink)
- LTE bandwidth mode: 20MHz
- LTE frame structure: currently fixed to TDD (configuration 5/5)

- Supported LTE physical channels and signals:
  - PSS – primary synchronization signals
  - CRS – cell-specific reference signals
  - PDCCH – Physical downlink control channel (with some proprietary modifications)
  - PDSCH – Physical downlink shared channel
- Configurable PDSCH parameters
  - MCS – modulation and coding scheme
  - PRB allocation (PRB group size 4)
- Simple PHY/MAC interface
  - Supporting applications like e.g. UDP video streaming
- Visualization capabilities/available KPIs
  - Display of Tx and Rx spectra
  - Display of PDSCH/PDCCH QAM constellations at the receiver
  - PDSCH/PDCCH BLER

As common for typical application software using the FPGA resources of NI's prototyping platform the described LTE application software consists of two major parts. One part comprises all real-time processing modules, which are implemented on the available FPGA resources using the LabVIEW FPGA programming capabilities. The other part is the so-called host application (written in standard LabVIEW). It is running on the PXIe controller in the PXI chassis (or alternatively on the processor of the connected laptop or standard PC). The main part of the LTE application software is the LabVIEW FPGA design implemented on the Kintex-7 FPGA of the USRP. It realizes the computationally intensive physical layer signal processing algorithms. As usual for such implementations, one top level LabVIEW FPGA module integrates all underlying sub-processing units. It also represents the interface to the host application. The host implementation realizes the control interface to the real-time FPGA implementation. It further provides the graphical user interface for the reconfiguration of the LTE transmission parameters, a simple PHY/MAC interface, and means to visualize Tx and Rx signal spectra as well as further receiver KPIs like e.g. QAM constellations and block error rates for the physical channels.

The parallel asynchronous 5G user is demonstrated by means of a real-time GFDM transmitter implementation running in parallel on a second USRP-2942R device. The RF Tx output signals of both USRP devices, i.e. of GFDM transmitter and LTE legacy transmitter, are combined by means of an RF coupler and the combined signal is finally fed into the Rx input of the LTE legacy receiver.
The GFDM transmitter implementation is realized by an adaptation of the LTE application software described above. Therefore, the OFDM modulator (IFFT + CP) of the LTE application software is replaced by a LabVIEW FPGA GFDM modulator implementation. The related software infrastructure and interfaces are adapted accordingly. Conceptually, the GFDM modulator implementation is based on the low complexity GFDM transmitter model and implementation proposal developed by the project partner TU Dresden (see section 4.1.1 for details). The implementation is realized in such a way that the GFDM modulator can also be configured to work as normal OFDM modulator. This eventually allows to directly evaluate the effects of an asynchronous GFDM user in comparison to the effects of an asynchronous OFDM user.

It should be noted, that for this demonstrator setup only the GFDM transmitter is implemented into the real-time software. The target scenario to be addressed by the described complementary real-time demonstrator is the co-existence of parallel asynchronous single user links in a fragmented spectrum use case with one link being an LTE legacy link and the other link using the OFDM or the non-orthogonal GFDM waveform. This scenario is exemplarily shown in Figure 5-13. The benefits of using the non-orthogonal waveforms for asynchronous transmissions can be verified by analyzing the

block error rate of the legacy link in a scenario with a secondary asynchronous user using either GFDM or alternatively simple OFDM as transmission waveforms.

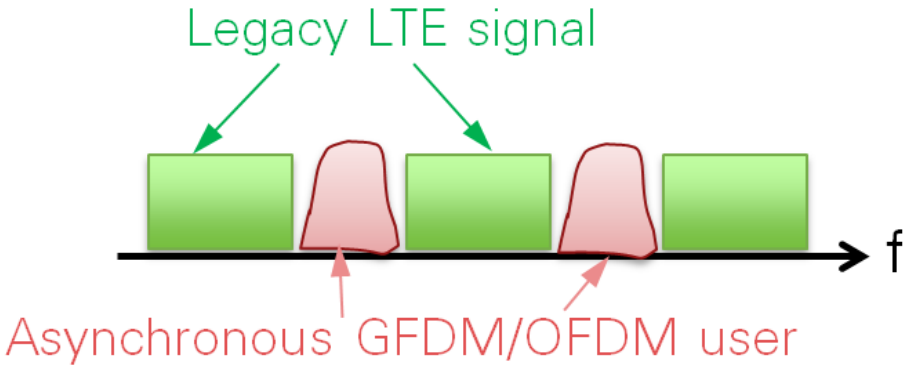


Figure 5-13 Target demonstrator scenario: LTE legacy link + asynchronous GFDM/OFDM user

6 Conclusion

This deliverable has presented the final demonstrator concept of the 5GNOW project, which is based on two main parts: GFDM transceiver and FBMC transceiver. The demonstrator concepts of the GFDM and FBMC transceivers represent hardware- and software prototype implementations of the respective non-orthogonal waveforms. They demonstrated the feasibility of the proposed waveforms as proof-of-concept using state-of-the-art RF platforms.

The deliverable has reminded two main scenarios, i.e. low latency and fragmented spectrum access, as a motivation and starting point for the two proposed waveforms. For the low latency scenario, the main key characteristics of GFDM together with a list of PHY parameters addressing this scenario were shown. For the fragmented spectrum access scenario, the FBMC concepts were explained and the corresponding PHY parameters were given. The next part of the deliverable presents the hardware platforms: the NI PXI platform provides a flexible and programmable environment that is, combined with the NI software development environment, used to implement the GFDM transceivers. For the FBMC implementation, baseband processing is done by dedicated baseband board developed by CEA-Leti and a specific daughter board that interconnects the baseband board with the NI PXI platform for over the air transmission.

Core part of the deliverable is the description of the final transceiver algorithms and control functionality. For the GFDM waveform, low complex transmitter and receiver approaches were given that enable to implement the GFDM approach in the FPGA of the NI PXI platform. For the FBMC transmitter and receiver, the implementation aspects of the baseband algorithms are summarized and complexity figures are given allowing some comparisons with OFDM transmitter.

The results presented in this deliverable are work-in-progress and therefore represent a snapshot of the current achievements. On the one hand, the complete base implementation verified that GFDM can be implemented with reasonable complexity using today's technology. On the other hand, practical implementations of FBMC in multiuser asynchronous frequency division multiple access mode were shown to be possible on Kintex-7 FPGA platforms. Future steps are planned for both considered waveforms. Especially joint demonstrations (either real time or non-real-time using HALO approach) will be carried out and the performance results of these joint demonstrators will be detailed in the upcoming deliverable D2.3.

The demonstrator platforms have been presented at several international conferences and workshops. The demonstrations assured the visibility of 5G-NOW in the scientific and industrial research community and gained valuable feedback. They also have significantly contributed to the ongoing discussions about 5G cellular systems by showing that non-orthogonal waveforms are not just theoretical concepts. Finally, demonstrators substantiate the theoretical efforts in the work packages 2-4 for the 5GNOW project internally and provided feedback regarding feasibility of the developed approaches and for their further improvement.

7 Abbreviations and References

3GPP	3rd Generation Partnership Project
4G	Fourth Generation
5G	Fifth Generation
5GNOW	5th Generation Non-orthogonal Waveforms for Asynchronous Signaling
ADC	Analog-to-Digital Converter
BER	Bit Error Rate
BS	Base Station
CoMP	Coordinated Multipoint
DAC	Digital-to-Analog Converter
EXALTED	Expanding LTE for Devices
FBMC	Filter Bank Multi-Carrier
FP7	7th Framework Programme
GFDM	Generalized Frequency Division Multiplexing
GSM	Global System for Mobile Communications
H2H	Human-to-Human
ICI	Inter-Carrier Interference
KPI	Key Performance Indicator
LTE	Long Term Evolution
LTE-A	Long Term Evolution Advanced
MAC	Medium Access (layer)
MTC	Machine Type Communication

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